IEEE Guide for the Application of Thyristor Surge Protective Devices

Sponsor

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Abstract: Applications information on fixed voltage and gated thyristor surge protective devices (SPDs) are provided. Key device parameters and their sensitivities are explained. Several worked telecommunication circuit design examples are given.
Keywords: application guide, telecommunication circuits, thyristor surge protection devices

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Introduction

(This introduction is not part of IEEE Std C62.37.1-2000, IEEE Guide for The Application of Thyristor Surge Protective Devices.)

This application guide has been produced as the companion to the IEEE Std C62.37-1996, IEEE Standard Test Specification for Thyristor Diode Surge Protective Devices (SPDs). The thyristor SPD parameters measured in IEEE Std C62.37-1996 are explained in terms of their application relevance and any operating condition sensitivities discussed. Several worked telecommunication circuit design examples are given, together with overviews of system problems, such as SPD coordination.

There are a very large number of thyristor SPD variants available. The two basic families of fixed-voltage and gated thyristor SPDs are further subdivided into bidirectional and unidirectional types. This guide provides information on these different types and the applications that they are most suited to. Substantive annexes provide information on design approaches, SPD technologies, device symbols, and equipment standards.

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IEEE Guide for the Application of Thyristor Surge Protective Devices

1. Scope

This application guide applies to thyristor surge protective device (thyristor SPD) components used in systems with voltages up to 1000 V rms or 1200 V dc. These components are designed to limit overvoltages and divert surge currents by voltage clamping and crowbarring (switching to a low impedance) actions. Although telecommunication circuits are the main application of thyristor SPDs, this guide will also provide useful information for other protection applications.

This guide is intended to complement the IEEE Standard Test Specification for Thyristor Diode Surge Protective Devices (IEEE C62.37-1996). The definitions used in these two standards are the same.

This publication contains information on

a) Basic function and component description
b) General terms and definitions
c) Electrical environment
d) Parameter interpretation and application
e) Example designs
f) SPD technology comparison

When used in conjunction with IEEE Std C62.37-1996, this guide will give the user guidance in interpreting its specifications and in selecting the correct product.

2. References

This guide shall be used in conjunction with the following publications:

IEC 60050-191 (1990-12): International Electrotechnical Vocabulary (IEV)—Chapter 191: Dependability and quality of service.[1]

[1]IEC publications are available from IEC Sales Department, Case Postale 131, 3, rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse. IEC publications are also available in the United States from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA.

IEC 61000-4-5 (1995-03): Electromagnetic compatibility (EMC)—Part 4: Testing and measurement techniques—Section 5: Surge immunity test.

IEEE C62.37-1996, IEEE Standard Test Specification for Thyristor Diode Surge Protective Devices.[2]

IEEE C62.41-1991 (Reaff 1995), IEEE Recommended Practice on Surge Voltages in Low-Voltage AC Power Circuits.

IEEE C62.42-1992 (Reaff 1999), IEEE Guide for the Application of Gas Tube Arrester Low-Voltage (Equal to or Less than 1000Vrms or 1200 Vdc) Surge-Protective Devices.

3. Definitions

For the purpose of this guide, the following definition has been used in addition to those in IEEE Std C62.37-1996 and *The Authoritative Dictionary of IEEE Standards Terms* [B8][3].

3.1 anti-parallel (connection): A parallel combination of two semiconductor elements, where the main current entry electrode of one element connects to the main current exit electrode of the other element, allowing one element to pass current in one voltage polarity and the other element to pass current in the opposite voltage polarity. (*syn:* **inverse-parallel connection** in IEEE 100 [B8])

4. Basic function and component description

This clause covers the basic device structure, its equivalent circuit, characteristic values, operational parameters, and structures with increased functions.

4.1 Basic device structure

Thyristor overvoltage protectors are manufactured by creating a series of N-type and P-type layers in a silicon chip. The basic thyristor structure has three PN junctions that require four layers (NPNP). As one layer can be the starting silicon itself (N or P-type silicon) a further three layers have to be made.

Figure 1 shows the simplified structure of a unidirectional thyristor SPD. The switching quadrant (see Figure 3) occurs when the bottom contact is positive with respect to the top contact. Also shown are the lumped equivalent circuit elements created by the semiconductor layers. This example started manufacture with an N^- slice of silicon. Layers of P material are then created at the top and the bottom. A further N^+ region is then made on the top surface. Finally the top and the bottom metallization are added to provide contacts. The upper right section of the contact metal is not shown in order to illustrate the detail of the topside silicon surface.

4.2 Device equivalent circuit

In Figure 1, transistor TR1 is formed by the N^+PN^- layers. Similarly transistor TR2 is formed by the PN^-P layers. The device breakdown voltage is determined by the breakdown of the central N^-P layers, which form a shared collector-base junction for transistors TR1 and TR2. For clarity, the breakdown function is shown as breakdown diode D1. Resistance R1 is the lateral resistance of the P layer. Resistor R2 together with resistor R1 shunt the base-emitter junction of transistor TR1 to define the value of holding current, I_H.

[2]IEEE C62.41-1991 (Reaff 1995), IEEE Recommended Practice on Surge Voltages in Low-Voltage AC Power Circuits.
[3]The numbers in brackets refer to the bibliography listed in Annex E.

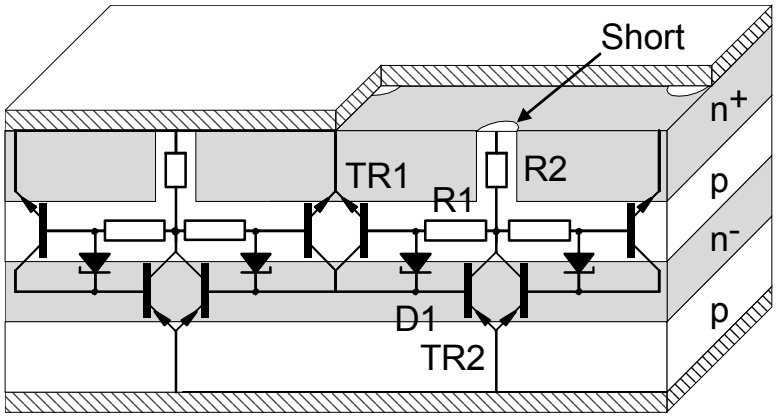

Figure 1—Simplified thyristor SPD

Resistor R2 has a relatively low value of resistance and is considered as a localized short circuit between base and emitter. During the manufacturing process, the emitter N^+ diffusion is perforated with a series of dots to create these short circuits. In Figure 1, some of the top metallization has been omitted to show the P-type shorting dots.

Figure 2 shows how the lumped circuit elements are equivalent to a thyristor. Transistors TR1 and TR2 are connected as a regenerative pair. In an unbiased condition, these transistors will be in an off state and present a high circuit impedance. If sufficient positive voltage is applied, diode D1 will break down and supply current to the transistor base regions. Initially, only transistor TR2 will conduct as the base-emitter shunt resistance of transistor TR1 will bypass the current. In this condition, the device voltage-current characteristic will be determined by the collector-emitter breakdown characteristic of transistor TR2. When sufficient current flows through the shunt resistance to initiate conduction of transistor TR1, the transistor pair will regenerate and switch (crowbar) to a low-voltage, on-state condition. The transistor pair will remain in this condition until the conducted current is too small to maintain sufficient voltage across the shunt resistance to activate transistor TR1. The current at which the transistor pair begins to switch off is called the holding current.

A simplified model of the lumped equivalent circuit replaces transistors TR1 and TR2 with a thyristor. This thyristor has a breakdown diode connected between its N-type and P-type gates and a resistive shunt between the P-type gate and cathode (see Figure 2). (An alternative version is possible with the resistive shunt between the N-type gate and the anode.)

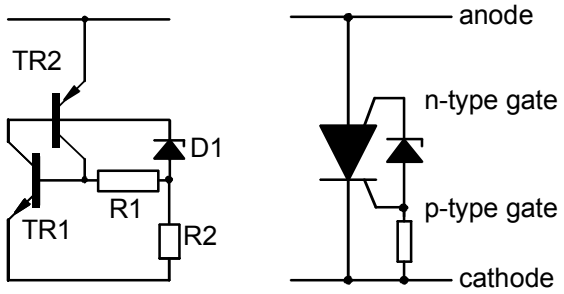

Figure 2—Lumped circuit and thyristor equivalent

4.3 Switching characteristics

The switching characteristic of a thyristor SPD consists of the following four regions:

a) Off-state
b) Breakdown
c) Negative resistance
d) On-state (see Figure 3)

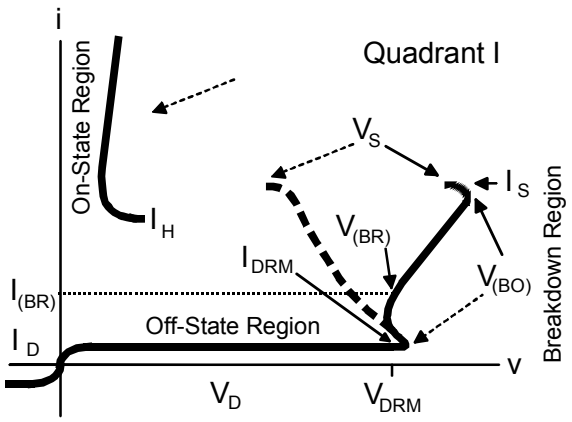

Figure 3—Thyristor SPD switching characteristic

4.3.1 Off-state region

The off-state region is the high-resistance, low-current portion of the voltage-current characteristic. This region extends from the origin to commencement of breakdown. The off-state current is the sum of junction reverse current and any surface leakage current. Two measurements are typically made in this region: off-state current (I_D), measured with the dc off-state voltage (V_D) applied; and repetitive peak off-state current (I_{DRM}), measured with the rated repetitive peak off-state voltage (V_{DRM}) applied.

4.3.2 Breakdown region

The breakdown region is the low-resistance, high-voltage portion of the voltage-current characteristic. This region begins where the low-current portion of the voltage-current characteristic changes from a high dynamic resistance to a region of substantially lower dynamic resistance for an increasing magnitude of current. Finally, this region terminates when sufficient thyristor regeneration occurs to initiate switching. Depending on the thyristor design and temperature, the end of the breakdown region may be at a higher or lower voltage than at the start. The low-resistance characteristic of this region is the result of junction breakdown combined with transistor action. The maximum voltage that occurs in the breakdown region is defined as the breakover voltage [$V_{(BO)}$]. Additional measurements may be made of the breakdown voltage [$V_{(BR)}$] at a given breakdown current [$I_{(BR)}$] and the voltage and current at the switching point [V_S , I_S].

4.3.3 Negative-resistance region

The negative-resistance region represents the trajectory from the breakdown region switching point to the on-state condition. This region is a dynamic condition, where the thyristor regeneration (internal positive current feedback) increases with time, causing an increased current demand that pulls down the voltage across the thyristor until the on-state condition is reached.

An overvoltage can be due to an impulse or a relatively long ac stress. The peak impulse let-though voltage will increase as the impulse rate of rise increases. Under ac surge conditions, heating and the resultant junction temperature rise increases the breakover voltage [$V_{(BO)}$]. At low currents, heating is due to breakdown region losses. At high currents, heating is due to on-state losses.

In telecommunication applications, there are two classes of protector—primary and secondary. Primary protection is applied at the system location where it may prevent most of the stressful energy from propagating beyond the designated interface. Secondary protection is applied subsequently to the primary protection and is subject to lower and better-defined stress levels. When a surge greatly exceeds the capability of a thyristor SPD it fails catastrophically, it may be desirable that the primary protector fails short circuit and so prevents the surge from propagating further. Primary protectors are normally tested to ensure their failure mode is appropriate to their application.

4.4.3 Durability

The thyristor SPD should have an adequate service life, and a design life in excess of 20 years is typical. Most of this period would be under normal operating conditions, and the product would have to pass a series of aggressive environmental tests to verify life expectancy. Surge conditions are a small, but significant, proportion of the service life. Surge durability is typically evaluated by repetitively surging the protector at various current levels.

4.5 Additional thyristor SPD structures

4.5.1 Gated thyristor SPD

These devices have a gate (G, g) terminal that controls the switching region characteristics, and two principal terminals provide the protective function. Three gate types are possible, as this additional terminal may be connected to either an intermediate P or N layer (Figure 4) of the thyristor SPD or a combined NP region (Figure 7). Some gated thyristor SPDs are designed to also allow operation without gate control. Without gate control the device operation and characteristics are the same as a fixed-voltage thyristor SPD (see 3.2).

In all gated thyristor SPDs, there will be the equivalent of a PNP transistor and an NPN transistor connected as a regenerative pair (Figure 4). In an unbiased condition, this transistor pair will be in an off state and present a high circuit impedance. The gate terminal layer and its adjacent principal terminal layer form a PN junction. When current is conducted by this PN junction, charge carriers are injected into the transistor pair. If sufficient gate current flows, the transistor pair will regenerate and switch (crowbar) to a low-voltage, on-state condition. The transistor pair will remain in this condition until the principal current is too low to maintain the conduction of the transistor pair.

There are two possible current loops for the gate current. One exists when the circuit producing the gate current is connected to the gate and its adjacent principal terminal. The other exists when the circuit providing the gate current is connected between the principal terminals. When the thyristor SPD is in the off state, there will not be any substantial current flow directly between the principal terminals. In this condition, the current flow loop is completed by the circuit connected between the gate and its nonadjacent principal terminal. The current flow path is adjacent principal terminal, gate terminal, and through the gate network to the nonadjacent principal terminal.

The most common circuit use for these devices is in the common gate configuration. By biasing the gate with an external reference voltage, such as the protected integrated circuit (IC) supply voltage, the protection voltage will track the value of the reference voltage. A P-gate device, with the gate biased negatively with respect to the anode, will provide negative transient voltage protection with respect to the anode. Similarly, an N-gate device, with the gate biased positively with respect to the cathode, will provide positive transient voltage protection with respect to the cathode.

These devices can also be current triggered in a conventional manner. In some cases, this is done by connecting the gate and adjacent electrode in series with the protected line wire.

4.5.2 Unidirectional blocking thyristor SPD

The switching quadrant performance of this device structure (Figure 4) is covered in 4.3. The inherent (fixed) voltage breakdown can be lowered by gate control, either by use of a single gate or both together. In the non-switching quadrant, current flow will be blocked by the reverse-biased $N^{-}P$ anode junction.

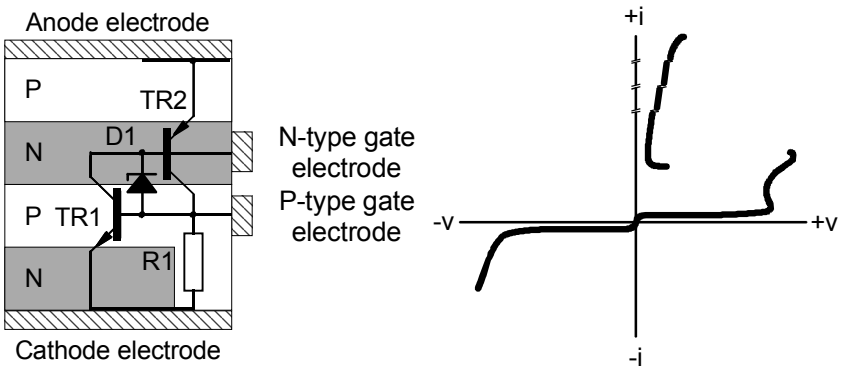

Figure 4—Unidirectional blocking thyristor SPD

4.5.3 Unidirectional conducting thyristor SPD

The switching quadrant performance of this device structure (Figure 5) is covered in 4.3. The inherent (fixed) voltage breakdown can be lowered by gate control, either by use of a single gate or both together. In the non-switching quadrant, current will be conducted by the forward-biased PN diode.

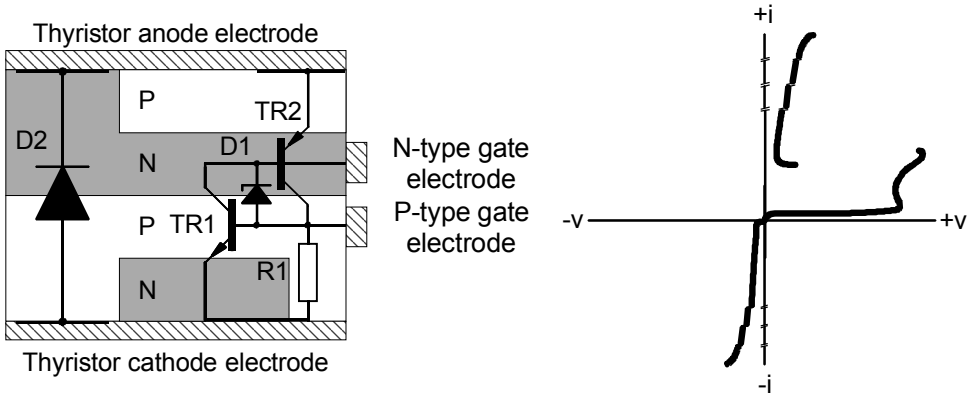

Figure 5—Unidirectional conducting thyristor SPD

4.5.4 Bidirectional thyristor SPD

This thyristor SPD has two unidirectional blocking thyristor SPD sections that are anti-parallel connected to give switching in quadrant 1 and quadrant 3 (see Figure 6). The inherent (fixed) voltage breakdown in each quadrant can be lowered by controlling the appropriate gate or gates.

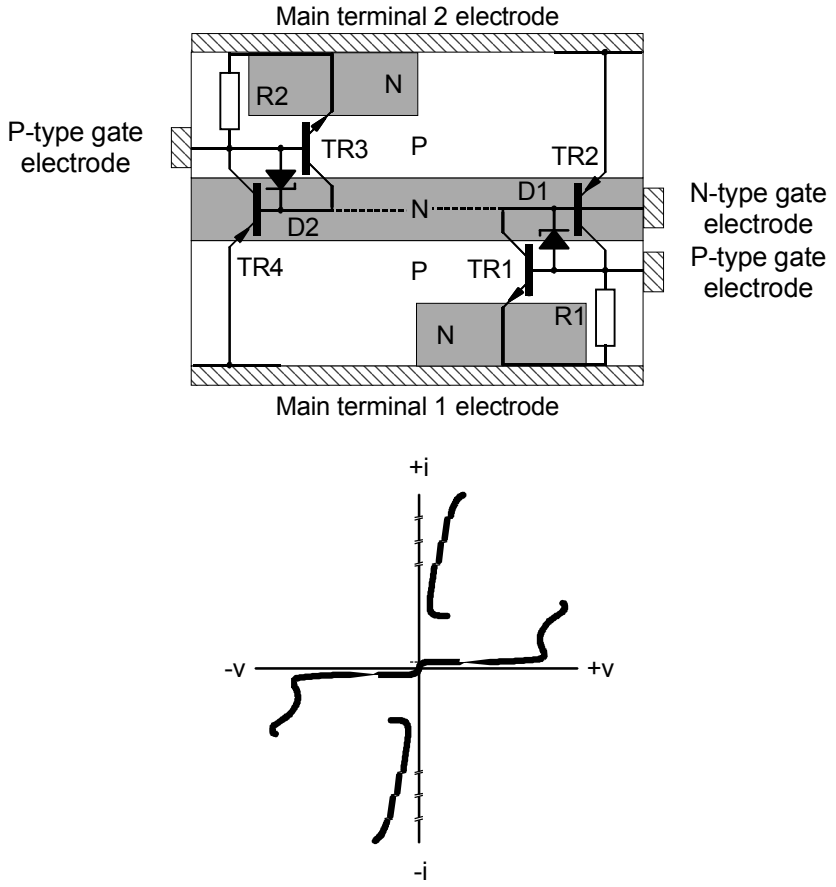

Figure 6—Bidirectional thyristor SPD

4.5.5 Bidirectional TRIAC thyristor SPD

This bidirectional thyristor SPD has a special gate structure (see Figure 7) that permits control in both quadrants with a single gate terminal. This is the standard TRIAC (TRIode for AC control) structure.

5. General terms and definitions

For the purposes of this guide, the definitions listed in 5.1 apply.

5.1 Types of thyristor SPD

The thyristor SPD is classified by the type of characteristic in quadrant 1 and in quadrant 3, and the number of terminals. At least one quadrant will have a switching characteristic (see Figure 8). The other quadrant may have a switching, blocking, or diode conduction characteristic (see Figure 8 and Figure 9). Devices with only one switching quadrant are called unidirectional and may have two (diode), three (triode), or four (tetrode) terminals. In addition, devices with two switching quadrants are called bidirectional and may have up to five (pentode) terminals (see Table 1).

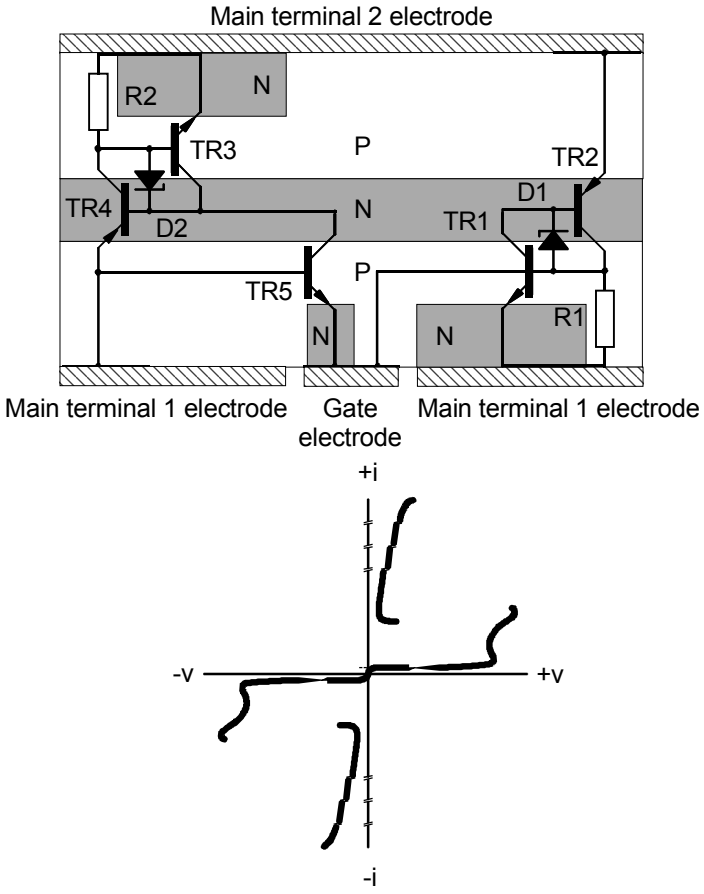

Figure 7—Bidirectional TRIAC thyristor SPD

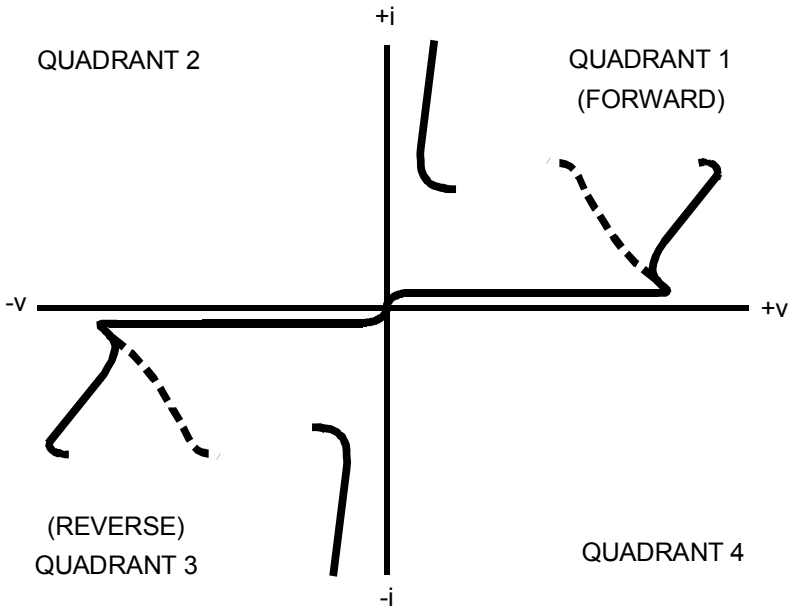

Figure 8—Switching characteristics in quadrant 1 and quadrant 3

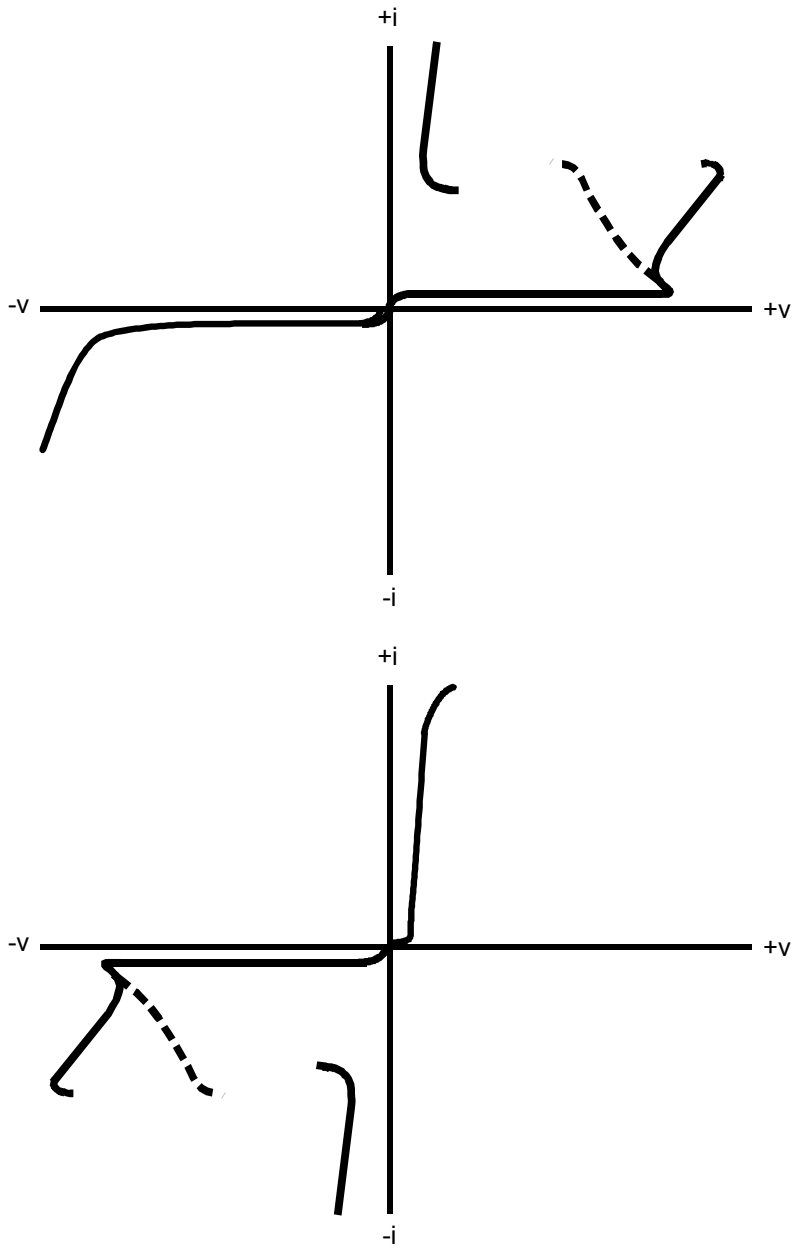

Figure 9—Examples of non-switching characteristics—reverse blocking in quadrant 3 and forward-conducting in quadrant 1

6. Electrical environment

Electrical and electronic systems and networks are subject to disturbances from external sources of electrical energy. These sources include electrical power circuits and natural phenomena, such as lightning. The effects of such disturbances may be confined to interference with normal use or operation, as in the case of noise or interference with signalling; or they may be capable of creating hazards to users and maintenance personnel or even damage to equipment. IEEE Std C62.42-1987 and IEEE Std C62.41-1991 contain further information on these environmental disturbances.

Table 1—Types of thyristor SPD

Number of terminals	Other quadrant characteristic		
	Blocking	**Conducting**	**Switching**
2 (diode)	Reverse-blocking or forward-blocking diode thyristor SPD	Reverse-conducting or forward-conducting diode thyristor SPD	Bidirectional diode thyristor SPD
3 (triode)	Reverse-blocking or forward-blocking triode thyristor SPD P-gate or N-gate	Reverse-conducting or forward-conducting triode thyristor SPD P-gate or N-gate	Bidirectional triode thyristor SPD P-gate or N-gate or combined P-gate and N-gate (TRIAC)
4 (tetrode)	Reverse-blocking or forward-blocking tetrode thyristor SPD P-gate and N-gate	Reverse-conducting or forward-conducting tetrode thyristor SPD P-gate and N-gate	Bidirectional tetrode thyristor SPD two gates
5 (pentode)			Bidirectional pentode thyristor SPD three gates

7. Parameter interpretation and application

This clause covers the relevance of thyristor SPD parameters to the system needs and details factors that affect those parameters. These parameters are grouped into the following three areas:

— Normal system operation
— Equipment protection
— Durability

7.1 Normal system operation parameters

These are parameters that affect the normal system operation. The thyristor SPD should not substantially interfere with the normal system operation; it should be transparent in normal system operation. Major performance areas are dc stand-by current, capacitive shunt impedance effects, distortion through signal clipping and restoration of service after an overvoltage.

7.1.1 Off-state current—I_D

Off-state current is the dc stand-by current that flows through the thyristor SPD when a dc voltage, V_D, is applied. The value of the applied test voltage, V_D, should be the same as the mean dc voltage level of the system. In many telecommunication systems, this would be the battery voltage level, which is typically – 50 V.

Figure 10 shows the typical temperature variation of off-state current. The off-state current has two components—a leakage current across the chip surface and an internal reverse current that flows through the chip's blocking junction. Surface leakage increases slowly with increasing temperature. Reverse junction current increases rapidly with temperature, more than doubling with every 10 °C rise.

Figure 10 shows that surface leakage current predominates at low temperatures and reverse junction current dominates at high temperatures. The crossover temperature of these two components depends on the chip size and surface quality.

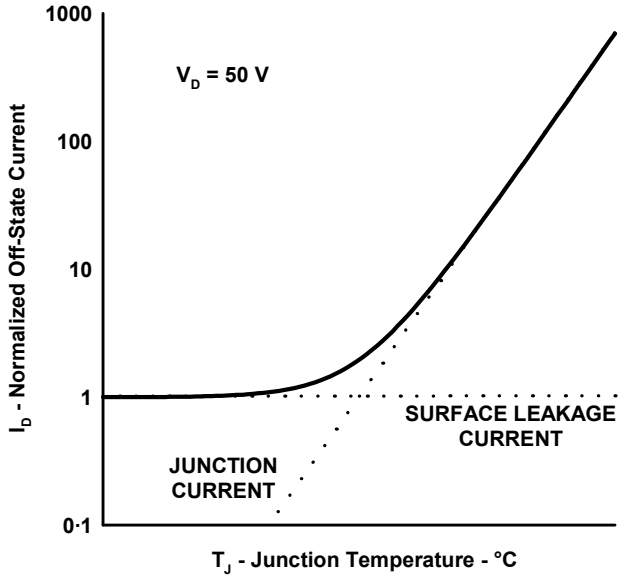

Figure 10—Normalized off-state current versus temperature

The test conditions for this parameter should specify the mean system dc voltage (V_D) and the highest system ambient temperature (T_A). In some systems, the mean system dc voltage may vary considerably from its nominal value, e.g., during battery charging, and this will affect the choice of the V_D value. Gated devices will need to have the gate terminal bias condition specified for this test.

Gated devices will also need the gate terminal dc stand-by current specified. Normally, a gate terminal junction will be reverse biased and have a characteristic similar to Figure 10. Measurement conditions should be specified similar to V_D. Current will be measured between the gate and one principal terminal. The measurement conditions should also include the condition of the other principal terminal (I_{GAS}, I_{GAO}, I_{GKS}, I_{GKO}). See IEEE Std C62.37-1996.

7.1.2 Repetitive peak off-state voltage—V_{DRM}

Repetitive peak off-state voltage is the maximum system voltage that can be applied to the thyristor SPD over a specified temperature range without the onset of clipping. Clipping causes system current to be diverted through the device.

Repetitive peak off-state voltage is a rating and is tested by applying V_{DRM} to the protector and measuring the resultant current that flows through the thyristor SPD. This voltage rating should be equal to or greater than the peak system operating voltage. In most analog telephone systems, the maximum voltage will occur during ringing, but occasionally maintenance test voltages may be higher.

Figure 11 shows how the single temperature value of V_{DRM} varies with temperature. The 25 °C value is normalized to unity. V_{DRM} is typically made up of an ac voltage with a dc voltage component. As the peak, repetitive off-state current is typically of the microampere order, the resultant power loss with V_{DRM} applied is very small. Practically, this makes the device junction temperature, T_J, rise above the local ambient temperature, T_A is very small. Under these circumstances, T_J and T_A can be regarded as equal in value. Figure 11 shows that V_{DRM} decreases with decreasing temperature and the lowest value will be at low temperatures. The critical value for V_{DRM} is at the lowest device (ambient) temperature, and it should be equal to or greater than the maximum system voltage.

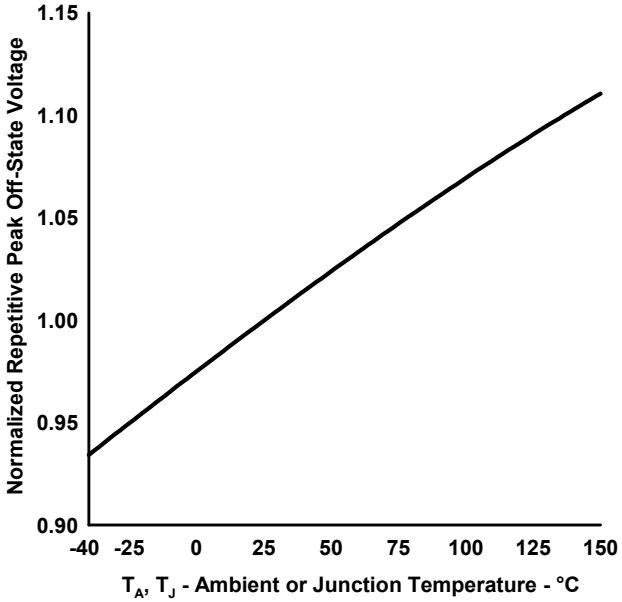

Figure 11—Normalized off-state voltage versus temperature

If the lowest temperature was 0, the V_{DRM} would have fallen to 0.975 of the 25 °C value. If the maximum system voltage was 200 V, V_{DRM} should be 200 V at 0 and the 25 °C verification check should be at 200/ 0.975 = 205 V (measured at 25 °C). If the lowest device temperature was –40 °C, the values become 0.94 and 213 V.

The test conditions for repetitive peak off-state current should specify the maximum system peak voltage (= V_{DRM} rating) and the system ambient temperature range (T_{AMIN} to T_{AMAX}).

For gated devices, this parameter may be covered by the V_D specification. Alternatively, these devices may be verified for V_{DRM} with the gate terminal open ($I_G = 0$) or connected to the appropriate principal terminal.

7.1.3 Critical rate of rise of off-state voltage—*dv/dt*

This is the maximum rate of rise of voltage that can be applied to the thyristor SPD over a specified temperature range without causing the device to switch on. The thyristor SPD should not switch on as a result of large *dv/dt* transitions that occur during normal system operation. In many telephone systems, these transitions do not exceed 50 V/µs. In such cases, a device *dv/dt* value of above 50 V/µs would give satisfactory performance. In addition, transition excursion would need to be in excess of at least 5 V to cause internal junction conduction. High *dv/dt* values of 1 kV/µs or more only reflect the inherent thyristor SPD technology, rather than a system need.

The device *dv/dt* rating should be based on the maximum system *dv/dt* applied as a ramp having an amplitude limited to the V_{DRM} value. In addition, gated devices will need to have the gate terminal bias condition specified.

7.1.4 Breakdown voltage—$V_{(BR)}$

This is a measure of the thyristor SPD voltage limiting at breakdown currents of a few milliamperes. It is comparable to the breakdown voltage of zener and avalanche diodes. If normal system operation causes device breakdown, system voltages will be clipped (limited), resulting in distortion and causing current

diversion through the thyristor SPD. In the telephone system, this action may cause equipment malfunction (e.g., false off-hook detection).

The preferred parameter for ensuring that the system voltages are not clipped is V_{DRM}. However, there has been a historical use of $V_{(BR)}$ (often called V_Z in older specifications) and the purpose of this clause is to provide background information. The breakdown voltage parameter is only used for fixed voltage, positive breakdown slope thyristor SPDs. It is inappropriate for fixed-voltage, negative breakdown slope and gated thyristor SPDs. These devices are specified by a V_{DRM} value and not by $V_{(BR)}$.

Breakdown voltage is a characteristic and is determined by applying a defined current to the device and measuring the resultant voltage. Test current levels in the range of 1 to 20 mA are typical. If $V_{(BR)}$ is specified, the minimum breakdown voltage value should be greater than the normal peak system operating voltage over the device temperature range.

Figure 12 shows how an avalanche breakdown voltage varies with temperature. The 25 °C value is normalized to unity. Figure 12 shows that $V_{(BR)}$ reduces with decreasing temperature and that the lowest value will be at low temperatures. The critical value for $V_{(BR)}$ is at the lowest device temperature, and it should be greater than the maximum system voltage by a few percent.

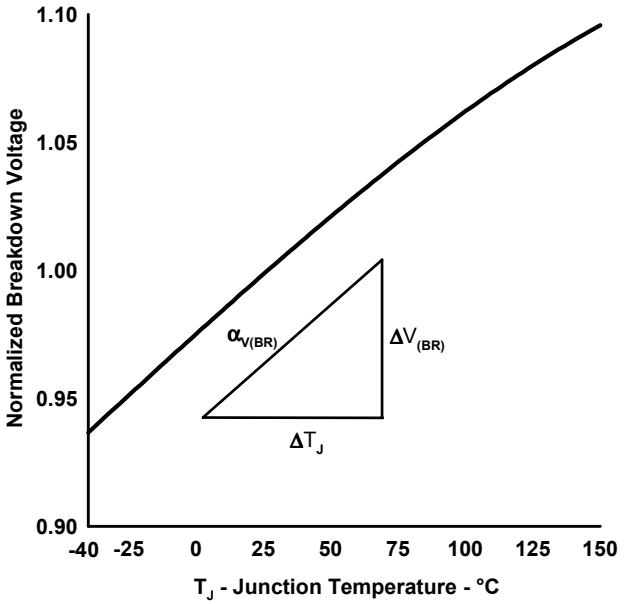

Figure 12—Normalized breakdown voltage versus temperature

The test conditions for breakdown voltage should specify the test current to be applied and the test temperature. If the test temperature is higher than the lowest system ambient temperature, the breakdown voltage temperature coefficient is required [$\alpha_{V(BR)}$ as shown in Figure 12]. The breakdown temperature coefficient will enable the calculation of the breakdown voltage at the lowest expected system ambient.

In most cases, the $V_{(BR)}$ parameter can be replaced by the same value V_{DRM} rating.

7.1.5 Holding current—I_H

This is a measure of the minimum current that will maintain the thyristor SPD in conduction after it has been switched to the on state. To ensure that the thyristor SPD switches off and restores normal system operation, the holding current must be greater than the maximum system dc short-circuit current.

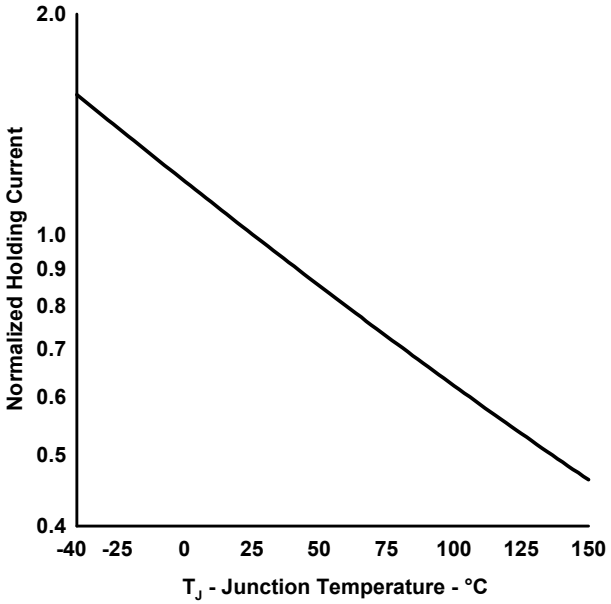

Figure 13—Normalized holding current versus temperature

Holding current is measured by switching the thyristor SPD to the on state and then reducing the on-state current until the device switches off. The current level that causes the device to switch off is taken as the holding current value.

Figure 13 shows that the holding current decreases with increasing temperature and that the lowest value will be at high temperatures. The critical value for I_H is at the highest device temperature, and it should be equal to or greater than the maximum system short-circuit current. At 70 °C, the holding current is about 0.7 of the 25 °C value.

In some cases, a temperature correction is required to allow for conduction losses. For example, consider the following parameters; system short-circuit current 100 mA, ambient temperature 70 °C, device on-state voltage 2 V, and device thermal resistance 60 °C/W. The device on-state dissipation would be 2 V × 0.1 A = 0.2 W, leading to a temperature rise of 0.2 W × 60 °C/W = 12 °C. So the holding current should be specified as 100 mA minimum at 70 °C + 12 °C = 82 °C junction temperature.

The measured holding current value will reflect the residual temperature due to the previous heating history. It is important not to have large dissipation prior to measuring holding current, otherwise the holding current value will be reduced. Holding current has a minor sensitivity (<10%) to circuit resistance. It is the interaction of circuit source resistance and the shape of the thyristor SPD on-state characteristic that determines the switch-off (holding) current. The measured holding current decreases as the source resistance increases. The test conditions for holding current should specify the on-state current, the current ramp down rate, source resistance, and the maximum junction temperature. The measured holding current value should be greater than the maximum system short-circuit current.

For gated devices, gate terminal conditions will need to be specified.

7.1.6 Capacitance—C_O

The junctions, formed by the device NPNP structure, are the principle elements that define the device capacitance. The capacitance of a PN junction will depend on the applied dc bias, V_D; ac test signal level, V_d; and junction temperature, T_J.

Figure 14 shows how the capacitance of a bidirectional thyristor SPD varies with dc bias and ac test level. For this figure, the capacitance values are normalized to the $V_D = 0$ and $V_d = 1$ V rms value. At low levels of dc bias, where the ac test level is significant compared with the dc bias, the capacitance is strongly dependent on the value of ac test level. The effective capacitance value decreases as the ac test level increases.

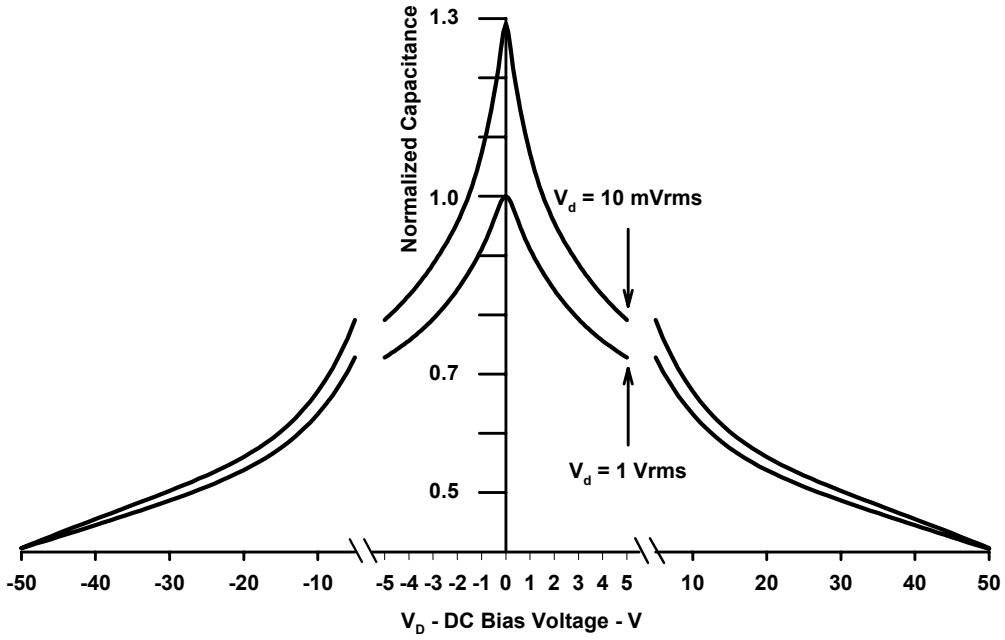

Figure 14— Normalized capacitance versus dc bias and ac test voltage

At high levels of dc bias, where the ac test level is insignificant compared with the dc bias, the capacitance is independent of the value of ac test level. Figure 14 shows a symmetrical capacitance characteristic. Devices with asymmetrical structures, such as planar types, have asymmetrical capacitance characteristics.

Measurement conditions are important for the case of two conductor balanced lines with a thyristor SPD, Th1 and Th2, from each conductor to ground (Figure 15). If the two conductors are dc biased at different levels, the device capacitance values will be different. This difference in capacitance values will create capacitive line unbalance. For example, from Figure 14, a device with a 100 pF zero bias capacitance (V_d = 1 V rms) would have capacitance values of 73 pF (100 pF × 0.73) and 40 pF (100 pF × 0.4) when biased at conductor voltages of –5 V and –50 V. This would create a capacitive unbalance of 33 pF, which for frequencies up to 1 MHz will not cause a problem.

Unidirectional conducting thyristor SPDs have the additional consideration of forward-biased diode conduction at low levels of dc bias. If the combination of dc bias and ac test level causes the diode conduction threshold to be exceeded, the diode will limit the voltage levels. Diode clipping (rectifying) the voltage will create harmonics, and often the measurement equipment will produce erroneous values (even changing from capacitive to inductive values). To measure such devices at near zero dc bias levels, the ac test level must be 100 mV rms or less.

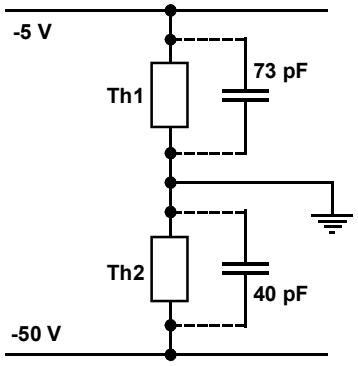

Figure 15—Capacitive line unbalance

Gated devices will have an additional capacitance from the principal terminals to the gate terminal. In many cases, the gate terminal will be ac grounded by a decoupling capacitor. This places the gate capacitance in parallel with the principal terminal capacitance. The principal terminal capacitance measurement method may include this gate capacitance. If the gate capacitance is guarded out of the principal terminal measurement, a separate measurement of the gate capacitance is required, which is then added to the appropriate principal terminal value. The gate should be biased at its normal system operating voltage(s).

Frequency usually has little impact on the capacitance value. Capacitance variation with frequency is usually due to measurement equipment problems or connection inductance. Under bias, temperature has a minor effect on the capacitance (see Figure 16), but this temperature effect may need to be taken into account in systems where stable capacitance values are critical. To ensure that the correct working value of capacitance is measured, the test conditions should reflect the actual value(s) of system dc bias level, and use the same ac test amplitude as the system signal and the operating temperature range of the system.

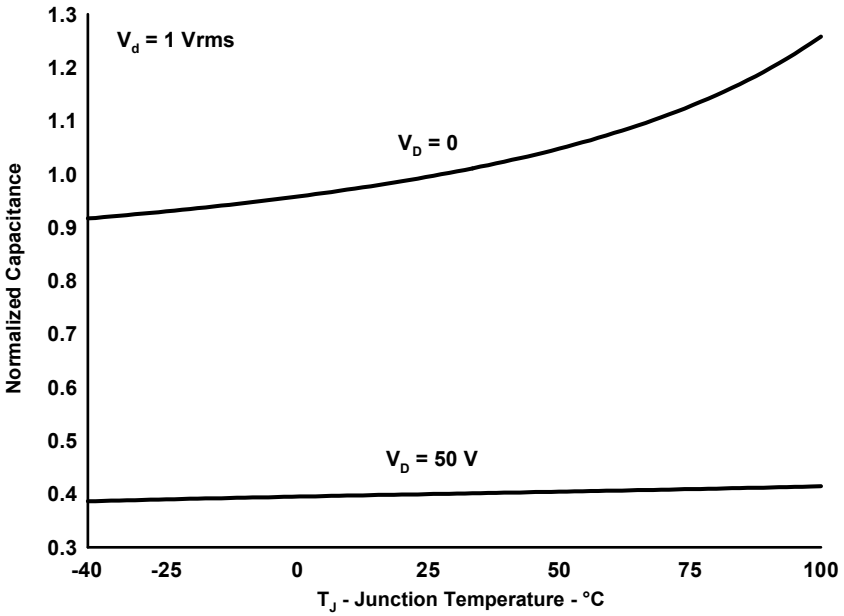

Figure 16—Normalized capacitance versus junction temperature

7.2 Equipment Protection Parameters

To protect the equipment against overvoltages, the thyristor SPD should limit the voltage to a level that does not cause equipment damage. The peak limiting voltage is the main criterion of protector performance under impulse and ac overvoltage conditions. In some cases, it is also important to know the time variation of the limiting voltage during the overvoltage condition.

7.2.1 Impulse overvoltage

The majority of impulse (lightning surge) generators produce double exponential waveforms. These waveforms have an exponential rise followed by an exponential decay.

Figure 17 shows a current impulse waveform. The virtual front time of the current impulse is defined as the zero-to-peak amplitude time of a straight line drawn through the 10% and 90% amplitude points on the front edge (1.25 times the time between the 10% and 90% points). The time at which the line crosses zero amplitude is called virtual origin. If the time between the 10% and 90% points was 6.4 μs, the virtual front time would be defined as 8 μs. The virtual time to half-value on the tail of the current impulse is the time between the virtual origin and the instant when the current has decreased to half (50%) its peak value. If the time between the virtual origin and the half-value point was 20 μs, the virtual time to half-value would be defined as 20 μs. An impulse with an 8-μs virtual front time and a 20-μs virtual time to half-value would be referred to as an 8/20 impulse (note that the μs time units are implied).

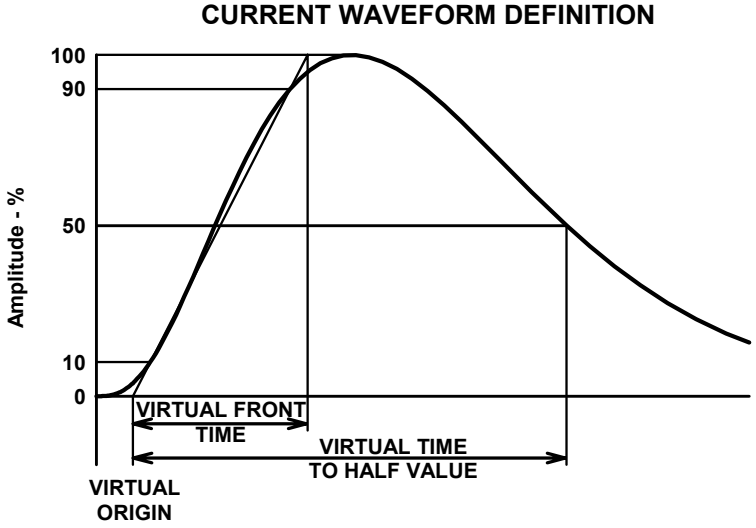

Figure 17—Current impulse waveform

In Figure 18, the virtual front time of the voltage impulse is defined as the zero-to-peak amplitude time of a straight line drawn through the 30% and 90% amplitude points on the front edge (1.67 times the time between the 30% and 90% points). The time at which the line crosses zero amplitude is called virtual origin. If the time between the 30% and 90% points was 0.72 μs, the virtual front time would be defined as 1.2 μs. The virtual time to half-value on the tail of the voltage impulse is the time between the virtual origin and the instant when the voltage has decreased to half (50%) its peak value. If the time between the virtual origin and the half-value point was 50 μs, the virtual time to half-value would be defined as 50 μs. An impulse with an 1.2-μs virtual front time and a 50-μs virtual time to half-value would be referred to as a 1.2/50 impulse (note that the microsecond time units are implied).

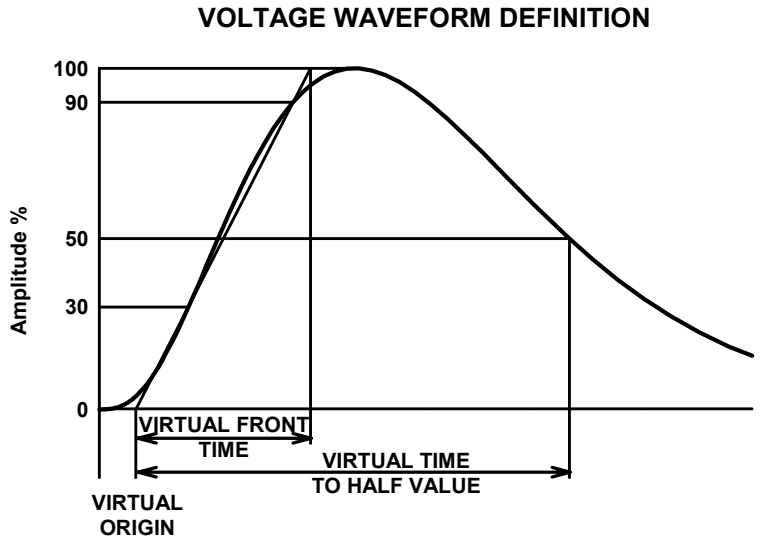

Figure 18—Voltage impulse waveform

Dividing of peak open-circuit voltage amplitude by the peak short-circuit current amplitude gives the generator fictive impedance. Fictive (effective) impedance is often used as the generator source impedance to calculate peak values of external load voltage and current.

There are three common types of impulse generator—circuit defined, waveform defined with similar voltage and current impulse wave shapes, and waveform defined with dissimilar voltage and current impulse wave shapes.

Figure 19 shows a "10/700" circuit-defined generator. IEC 61000-4-5 (1995-03) defines the open-circuit voltage waveform as having a front time of 10 μs ± 30% and a time to half-value of 700 μs ± 20%. The corresponding short-circuit current waveform would have a front time of 5 μs ± 30% and a time to half-value of 320 μs ± 20%

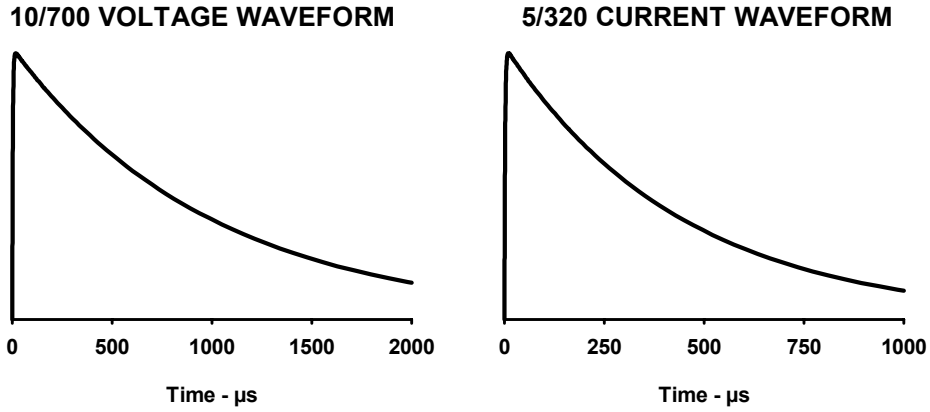

Figure 19—"10/700" generator waveforms

Figure 20 shows a "10/1000" waveform generator where the open-circuit voltage and short-circuit current waveforms are essentially the same. IEEE Std C62.41-1991 defines the open-circuit voltage waveform as having a front time of 10 μs + 0 μs – 5 μs and a half-value time of 1000 μs +1000 μs –0 μs. The short-circuit current waveform is defined as having a front time of 10 μs + 0 μs – 5 μs and a half-value time of 1000 μs ± 200 μs.

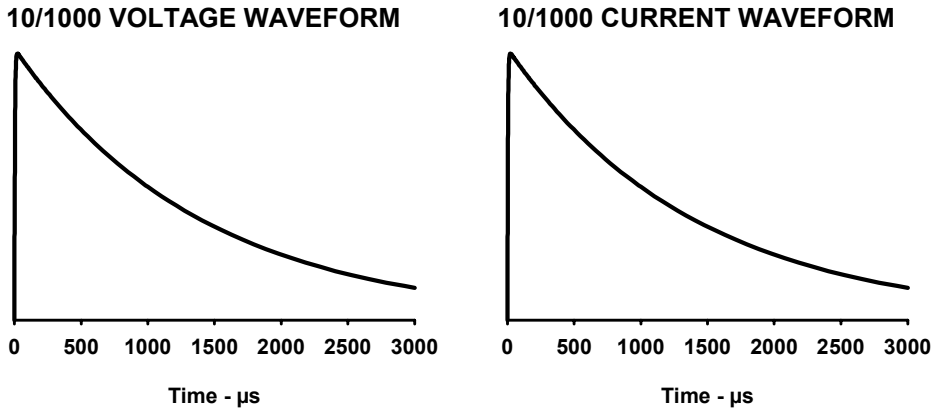

Figure 20—10/1000 waveforms

Figure 21 shows a "1.2/50 8/20" combination wave generator where the open circuit voltage and short circuit current waveforms are different. IEC 61000-4-5 (1995-03) and IEEE Std C62.41-1991 define the open-circuit voltage waveform as having a front time of 1.2 μs ± 0.36 μs and a half-value time of 50 μs ± 10 μs. IEC 61000-4-5 (1995-03) defines the short-circuit current waveform as having a front time of 8 μs + 1.0 μs – 2.5 μs and a time to half-value of 20 μs + 8 μs – 4 μs. The fictive source impedance of the generator is specified as 2.0 Ω ± 0.25 Ω. IEEE Std C62.41-1991 defines the short-circuit current waveform as having a front time of 8 μs ± 20% and a time to half-value of 20 μs ± 20%.

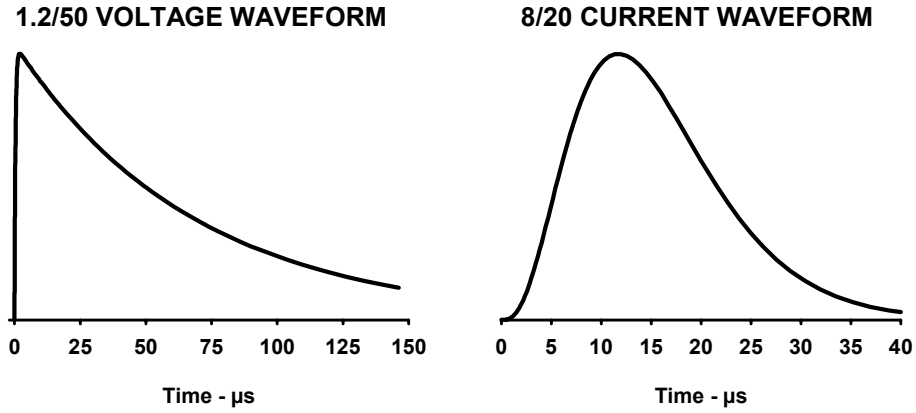

Figure 21—1.2/50 and 8/20 waveforms

7.2.1.1 Impulse breakover voltage—$V_{(BO)}$

Impulse breakover voltage is the peak value of device breakdown voltage when a defined impulse is applied. The $V_{(BO)}$ value depends on the initial device temperature and the rate of rise of breakdown current. The rate of rise of current is a function of the impulse generator, any series circuit impedances, and the dynamic

breakdown slope impedance of the thyristor SPD. Generally, the relevant value of *di/dt* will only be the initial rate of rise of current when the device is in the breakdown region and before switching occurs. The current impulse overall rate of rise may be slower or faster than the initial value.

At high rates of current rise, all thyristor SPDs will have positive slope impedances (Figure 22). This is due to the finite reaction time of the thyristor, which prevents the formation of negative breakdown slopes and delays the device switch on, resulting in higher values of breakdown current and voltage.

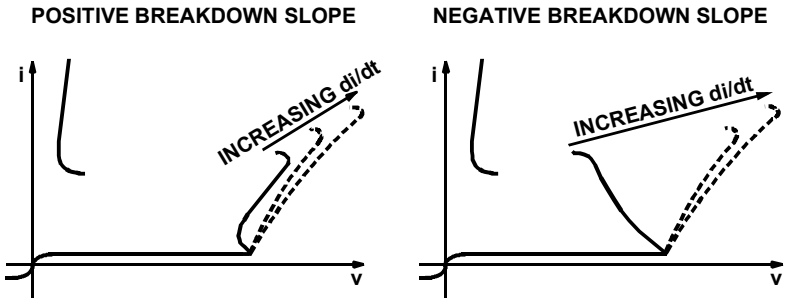

Figure 22—Increase in $V_{(BO)}$ due to di/dt

The change in $V_{(BO)}$ with increasing *di/dt* may be given as specific values or a graph. Figure 23 is an example graph of $V_{(BO)}$, normalized to the single-cycle 50/60-Hertz value, against *di/dt*. If the device 50/60-Hz $V_{(BO)}$ value was 200 V, an impulse with an initial *di/dt* value of 10 A/µs would result in an impulse $V_{(BO)}$ value of 1.05×200 V = 210 V.

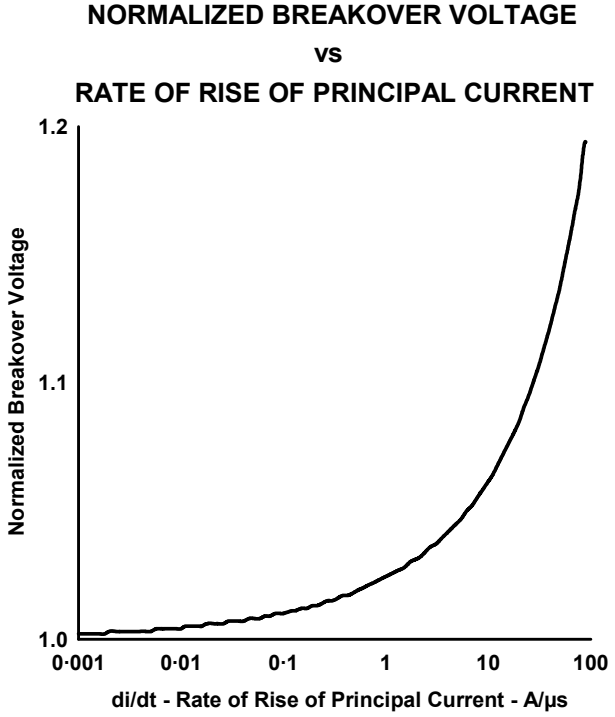

Figure 23—Increase in normalized $V_{(BO)}$ with di/dt

For telecommunication Subscriber Line Interface Circuit (SLIC) ICs, the voltage-limiting waveform may be just as important as its peak value [$V_{(BO)}$]. This type of requirement is usually expressed as a series of voltage-time windows which are referenced to ground and the SLIC supply voltage, V_{BAT}. In these cases, the entire voltage-limiting waveform must be contained within the voltage-time template. Figure 24 shows an example of such a template.

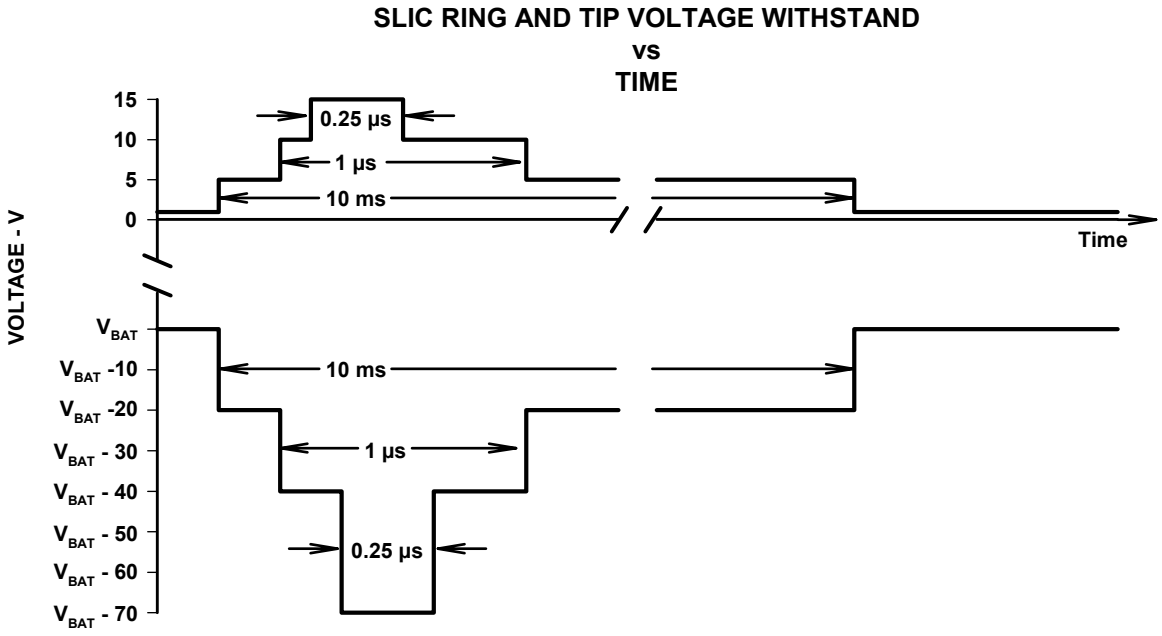

Figure 24—An example of SLIC voltage withstand

The test condition for $V_{(BO)}$ should be specified either by generator and circuit components or by the breakdown region *di/dt* value (limited to a peak current value), as well as by the required ambient temperature range.

Gated devices will need the gate conditions to be specified. In some cases it may be required to determine the peak gate current and the resultant gate charge, Q_{GS}. Both of these parameters may be given as specific values or as graphs against *di/dt*.

In Figure 25, the positive gate charge (Q_{GS}) is about 0.1 µC, which, with a 0.1-µF gate decoupling capacitor, would increase the gate supply by about 1 V (= 0.1 µC/0.1 µF). This increase does not directly add to the protection voltage as the supply voltage change reaches a maximum as the gate current reverses polarity; whereas the protection voltage peaks earlier than this. At the protection voltage peak, about half of the gate supply rail voltage increase will have occurred. In Figure 25, the peak clamping voltage [$V_{(BO)}$] is –77.5 V, an increase of 5.5 V on the nominal –72 V gate supply voltage. This 5.5 V increase is the sum of the supply rail increase (0.5 V) and the protection circuits gate-cathode breakover voltage (5.0 V). Faster *di/dt* impulses will cause larger values of Q_{GS}. The minimum value of a gate decoupling capacitor should be determined for the largest expected value of Q_{GS}.

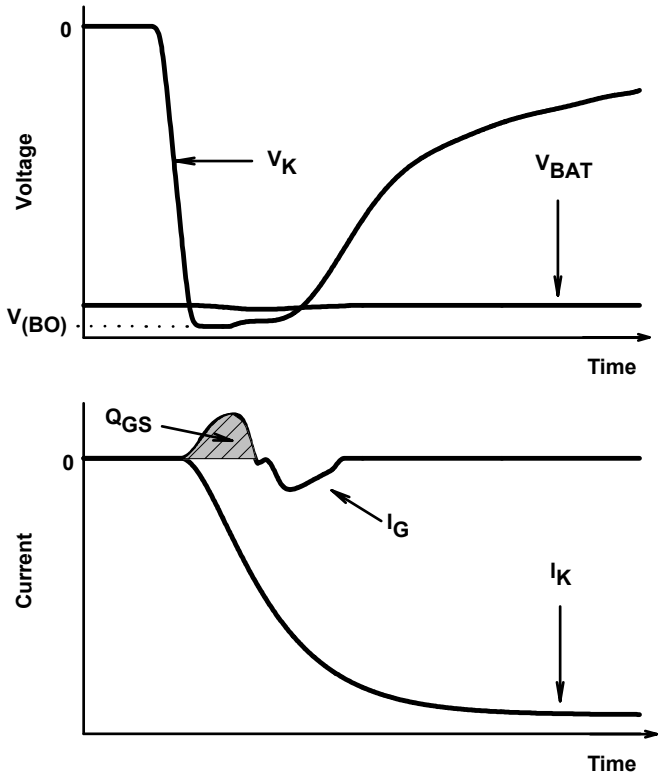

Figure 25—Gated protector, fast impulse clamping and switching waveforms

7.2.1.2 Impulse forward recovery voltage —V_{FRM}

This is the peak value of diode forward voltage when a defined impulse is applied (Figure 26). The V_{FRM} value depends on the initial device temperature and the rate of rise of forward current. The current rate of rise is a function of the impulse generator, any series circuit impedances, and the forward recovery characteristic of the diode. Generally, the relevant value of *di/dt* will be the initial rate of rise of current. The current impulse rate of rise calculated from the peak current and the wavefront virtual duration may be slower or faster than the initial value.

The change in V_{FRM} with increasing *di/dt* may be given as specific values or as a graph. Figure 27 is an example graph for V_{FRM}. Similar to $V_{(BO)}$, discussed in 7.2.1.1, the voltage-limiting waveform may be just as important as its peak value (V_{FRM}).

The test condition for V_{FRM} should be specified either by generator and circuit components or by the current *di/dt* value (limited to a peak current value), as well as by the required ambient temperature range.

7.2.2 AC overvoltage

AC overvoltages range in time from a few cycles to over 15 minutes. During this condition, the device temperature rise and consequent limiting voltage value will be dependent on the device power dissipation, and overall thermal impedance of the device and its mounting (see Figure 28). For short durations, the peak-limiting voltage will depend on the silicon chip and package performance. The package mounting (heatsinking) will greatly influence the peak-limiting voltage for long time periods of ac overvoltage.

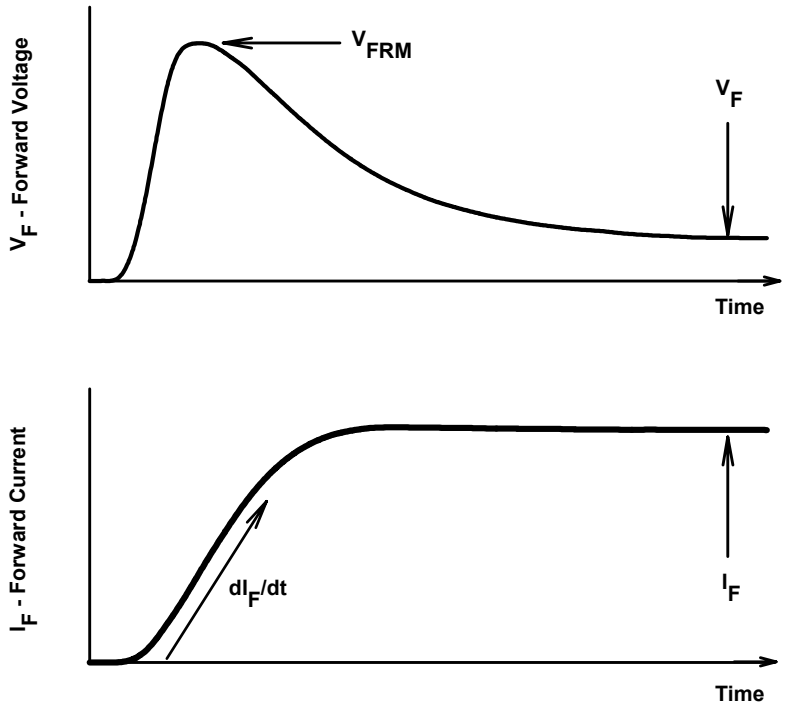

Figure 26—Forward recovery characteristic due to di_F/dt

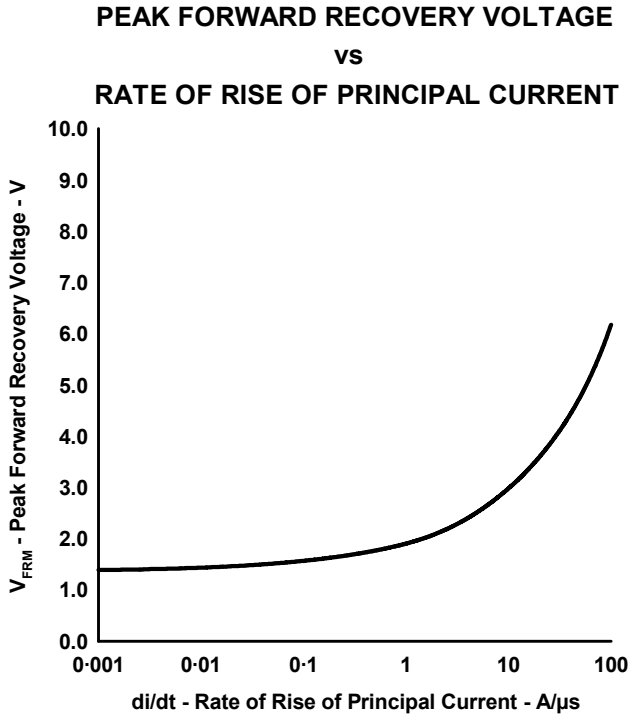

Figure 27—Increase of peak forward recovery voltage with *di/dt*

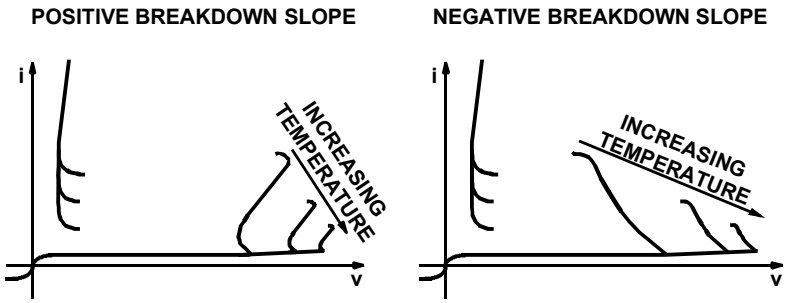

Figure 28—Peak voltage [$V_{(BO)}$] increase with increasing temperature

7.2.2.1 AC breakover voltage—$V_{(BO)}$

If the junction temperature increase, caused by ac heating, is sufficiently high, the maximum value of $V_{(BO)}$, measured under ac conditions, can exceed the value of $V_{(BO)}$, measured under impulse conditions. For fixed voltage devices with $V_{(BO)}$ values above 10 V, $V_{(BO)}$ will generally increase with temperature. The temperature behavior of $V_{(BO)}$ depends on where the breakover point occurs in the breakdown region (see Figure 29). If it occurs at the beginning of the breakdown region, giving $I_{(BO)}$ values typically below a few hundred microamperes, then, at high temperatures, the off-state current will have increased sufficiently to exceed the $I_{(BO)}$ value at which the $V_{(BO)}$ would normally occur. At this temperature and above, the rate of $V_{(BO)}$ increase would reduce, finally changing to a negative value, causing $V_{(BO)}$ to decrease with increasing temperature.

If $V_{(BO)}$ occurs toward the end of the breakdown region, giving $I_{(BO)}$ values typically above 100 mA, then the increase in $V_{(BO)}$ with temperature is reasonably linear. At very high temperatures (≈300 °C), the off-state current will have increased sufficiently to exceed the $I_{(BO)}$. At this temperature and above, the rate of $V_{(BO)}$ increase would reduce, finally changing to a negative value, causing $V_{(BO)}$ to decrease with increasing temperature.

Figure 30 plots an example of peak voltage [$V_{(BO)}$] per cycle against time for three levels of ac current. The device used had a single-cycle $V_{(BO)}$ value of 340 V. For the low current level, where the device does not switch and only operates in the breakdown region, the device temperature rise caused by heating is gradual. This is shown by a slow, progressive voltage rise from 356 V at 0.1 s to 372 V at 1000 s. After 300 s, the voltage is constant, showing that thermal stability has been reached.

Both high and medium currents cause the device voltage to peak and then collapse. In both cases, the heating is substantial, which raises the device junction temperature to a level where semiconductor junction action stops and the device becomes resistive. The high current condition starts at 351 V, and peaks at 383 V in 4 s before collapsing to 4 V. The medium current condition starts at 358 V, and peaks at 381 V in 25 s before collapsing to 2 V.

For the levels and times used for this example, the maximum $V_{(BO)}$ was 16% higher than the single-cycle value. In verifying the overvoltage protection, it is important to specify the ac voltage level, the application time, the overall circuit resistance, the device mounting arrangement, circuit connections, and any current-limiting components. The ac voltage and circuit resistance will determine the prospective on-state current, and the resulting losses in the breakdown and on-state conditions. The thermal characteristics of the mounting will influence the medium and long-term temperature rise, which will reflect in the $V_{(BO)}$ value. Circuit connections will determine whether single or multiple protectors are activated.

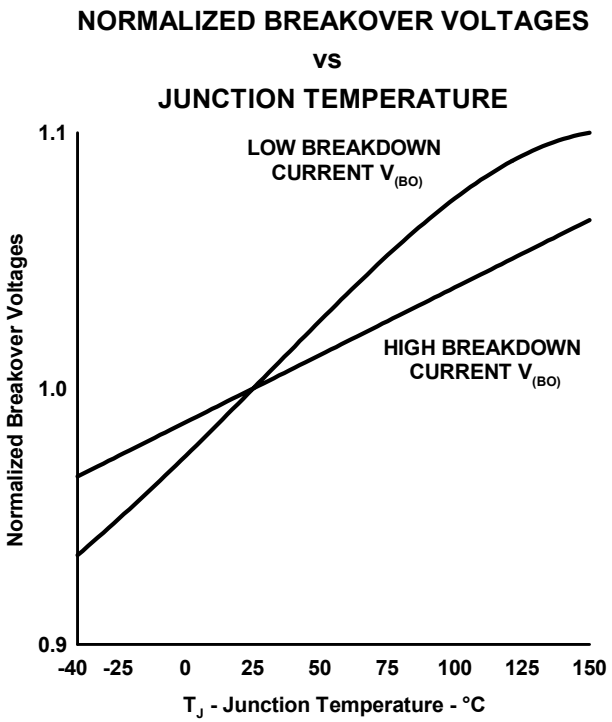

Figure 29—Breakover voltage variation with temperature

Current-limiting components may activate before the end of the specified test time. This will effectively shorten the test time and could reduce the peak voltage. When fusible current-limiting elements operate, the current flow will stop. When Positive Temperature Coefficient (PTC) resistors switch to a high resistance, the current flow greatly reduces. This condition needs to be evaluated. The low current can cause the thyristor SPD to be biased in the breakdown region. A combination of low current and high breakdown voltage can cause high dissipation, leading to a large voltage rise.

Gated protectors, where the gate is reference to a fixed voltage, show very little change in $V_{(BO)}$ until the temperature rise causes the semiconductor properties to be lost and the device turns resistive. In this condition, the gate will also become resistive and short out the gate supply voltage. To avoid excessive gate current flow, a series resistor or fusible element may be used in series with the gate. Alternatively, the circuit component values could be specified so that the protector does not reach a resistive condition.

Testing all possible combinations of ac power fault conditions is time consuming. Testing by computer simulation should comprehend device characteristics up to 300 °C, junction to ambient thermal impedance data, the test configuration, ambient temperature range, and the characteristics of any current limiters employed. For gated protectors, the gate losses in the triggering and any reverse current flow [I_{GAF}, I_{GKF}, I_{GAT}, I_{GKT} (see IEEE Std C62.37-1996)] need to be added. The reverse-current gate power will be dependent on the value of gate bias voltage. To maximize this power, the highest level of gate supply voltage should be used.

7.2.2.2 AC forward voltage—V_F

The (diode) forward voltage of a reverse- or forward-conducting thyristor SPD is the limiting voltage in that polarity. Under ac conditions, any changes in V_F due to current or temperature are usually insignificant compared with the impulse forward recovery voltage. It is usually sufficient to specify a forward voltage measured at 25 °C and the peak value of the maximum expected ac current.

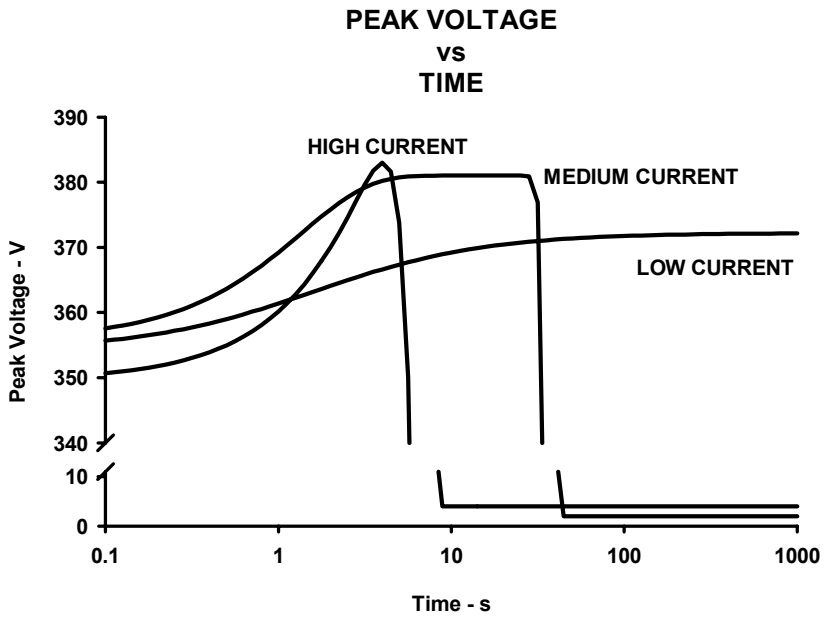

Figure 30—Peak voltage per ac cycle with time

7.3 Durability

The thyristor SPD should have adequate electrical and thermal ratings to ensure the required service performance. In addition, manufacturers should make available reliability data [e.g., 1000 hour High Temperature Reverse Blocking (HTRB) performance] to verify the product design integrity.

7.3.1 Maximum electrical and thermal ratings

Maximum ratings are limiting capabilities or limiting conditions beyond which damage to the device may occur.

7.3.2 Repetitive

A repetitive maximum rating may be applied continuously to the thyristor SPD without damage occurring to the device.

7.3.2.1 Repetitive peak on-state current—I_{TRM}

This is the steady-state ac capability of the thyristor SPD. The test conditions should specify the ac source voltage level, the source resistance, the device mounting arrangement, circuit connections, and ambient temperature(s). This rating is used to verify the device current capability for ac overvoltage tests lasting 300 s or more.

7.3.2.2 Repetitive peak off-state voltage—V_{DRM}

The value and application of this parameter are covered in 7.1.2.

7.3.2.3 Repetitive peak junction temperature—T_{JM}

The repetitive peak junction temperature value is used by the manufacturer as a limiting value to establish other repetitive ratings, such as I_{TRM}.

7.3.2.4 Storage temperature range—T_{stg}

The storage temperature range limits can be used by manufacturers as thermal-cycling temperature limits.

7.3.2.5 Thermal resistance—R_{theta}

The thermal resistance value can be used by the manufacturer as a limiting value to establish other repetitive ratings, such as I_{TRM}.

7.3.3 Nonrepetitive

A nonrepetitive maximum rating may be applied to the thyristor SPD for a minimum of 100 times over the life of the device without damage occurring. During this rated condition, the device is permitted to exceed its maximum-rated junction temperature for short periods of time.

7.3.3.1 Nonrepetitive peak on-state current—I_{TSM}

This rating can be expressed as specific peak ac current-time values or a graph. If the designer ensures that the thyristor SPD is always operating below this limiting capability, protector failure will not occur. The test conditions should specify the ac source voltage level, the source resistance, the device mounting arrangement, circuit connections, and ambient temperature(s). This rating is used as a design limit for the selection of other circuit components such as current limiters and resistors. Some ac tests are applied for 15 min, and so the rating curves should extend out to 1000 s (Figure 31).

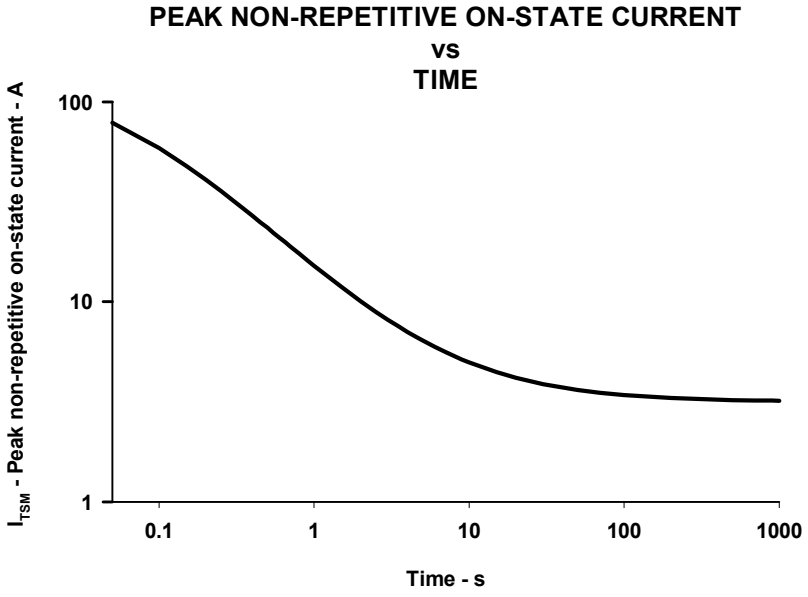

Figure 31—Peak nonrepetitive ac on-state current against duration

Peak nonrepetitive on-state current and ac $V_{(BO)}$ are two parameters determined from the same test conditions. Peak nonrepetitive on-state current is set by thyristor SPD survival. AC $V_{(BO)}$, 7.2.2.1, is set by the protected equipment voltage withstand capability. Designing with peak nonrepetitive on-state current values may result in ac $V_{(BO)}$ values that would cause equipment failure. In this case, the manufacturer should be requested to provide a derated curve which ensures that the required value of ac $V_{(BO)}$ is not exceeded.

7.3.3.2 Nonrepetitive peak pulse current—I_{PPS}

This rating can be expressed as specific peak impulse current-time values or with a graph. If the designer ensures that the thyristor SPD is always operated below this limiting value, protector failure will not occur. The test conditions should be specified by generator and circuit components, as well as by the required ambient temperature range. This rating is used as a design limit for the selection of other circuit components such as series resistors.

The thyristor (chip) impulse current diverting capability (without failure) reduces at both high and low temperatures. As the temperature increases, it takes less energy and, hence, current to raise the thyristor overall chip temperature to initiate failure. As the temperature decreases, the on-state current takes longer to uniformly distribute across the chip. If the impulse current rises at a fast rate, the current will not have time to propagate and will be concentrated in a small area. This localized power dissipation can lead to hot spots and cause device failure. Thus, as the propagation time increases, the ambient temperature decreases; this effect reduces the current capability at low temperatures on fast-rising impulses. In summary, when bulk energy capability is the cause of failure, increasing the ambient temperature will reduce the impulse current capability. When failure is caused by the chip current propagation speed, decreasing the ambient temperature will reduce the impulse current capability. There are other device failure mechanisms, e.g., the capability may be limited by the fusing of the package terminal to chip electrode connection.

Figure 32 is an example of how impulse current capability varies with wave shape designation and temperature. The capability is plotted as the cumulative population percentage on a probability scale. This scale has the advantage that a population with a normal distribution appears as a straight line. If the population distribution tail is reasonably straight, it can be extrapolated downward to predict peak current values for specified failure rates (0.1% would be 1000 ppm and 0.001% would be 10 ppm). In practice, the predicted current value would need to be derated by a further 10% to avoid physical deformation of the thyristor chip metallization caused by the high temperatures as the chip nears the failure point.

The 10/1000 wave shape is a relatively slow-rise, long-duration, high-energy impulse. As the current rate of rise is slow, the device current capability is determined by bulk energy. The various temperature populations run close together with the 85 °C ambient population being the lowest. The 2/10 is a fast-rise, short-duration, high rate-of-rise impulse. The device 2/10 current capability is higher than 10/1000, but the populations are wider apart and, at the lowest current levels, are in reverse temperature order compared with the 10/1000. At –40 °C, the device has the slowest propagation speed, and so this population has the lowest current capability. At 85 °C, propagation speed is not the major failure cause and the current capability is determined by bulk energy. The 25 °C population is a mixture of propagation and bulk energy failures. A major portion of the population has an appreciable propagation loss that lowers the current capability below the 85 °C levels. The remainder of the distribution is limited by bulk energy and so exceeds the higher value 85 °C current levels.

A diode does not have appreciable propagation loss; therefore, its capability will be set by bulk energy. For both waveforms, the highest capability occurs at the lowest temperature and the lowest capability occurs at the highest temperature (Figure 33).

The surge rating should only be specified for the system temperature range. Requesting a standard temperature range like –40 °C to 85 °C may needlessly increase the size of the protector.

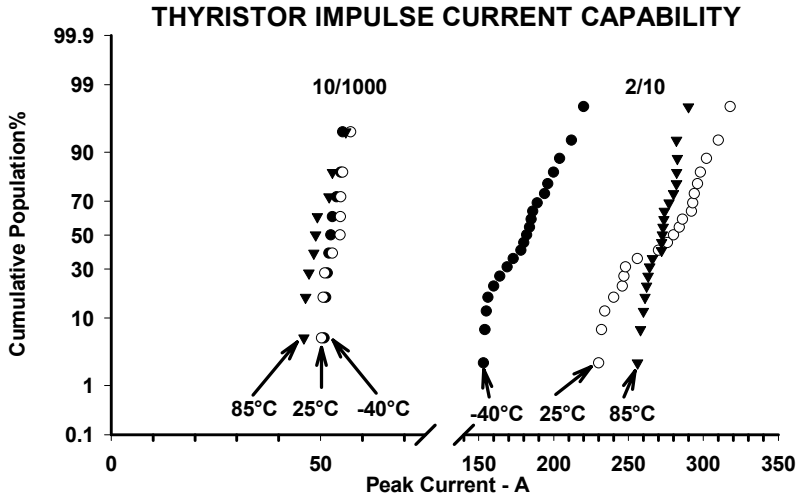

Figure 32—Example of thyristor 2/10 and 10/1000 impulse capability with temperature

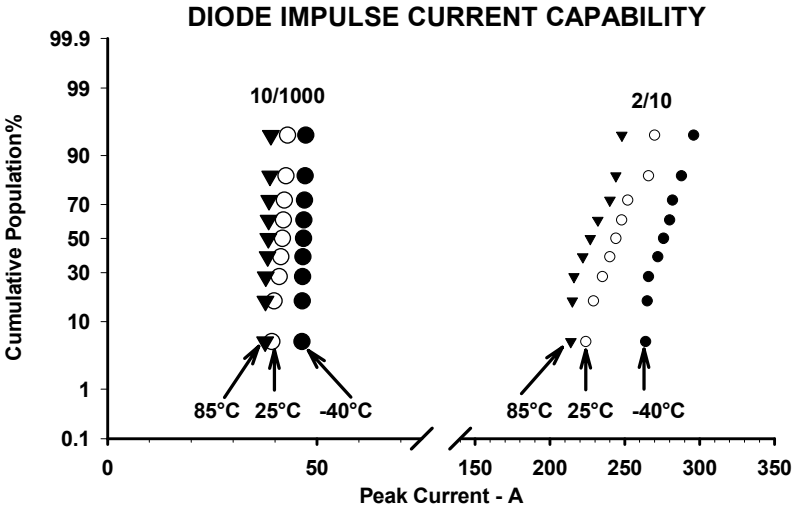

Figure 33—Example of diode 2/10 and 10/1000 impulse capability with temperature

7.3.3.3 Critical rate of rise of on-state current—*di/dt*

The premature failure caused by rapidly rising current impulses is discussed in 7.3.3.2. The *di/dt* capability must be at least equal to the that produced by the fastest rising impulse that the thyristor SPD is rated for. Verification of both impulse rating and *di/dt* rating can be done by applying this particular impulse.

7.3.3.4 Nonrepetitive peak gate current—I_{GSM}

On fast rising impulses, a large amount of current can flow out of the gate for short periods. The parameter Q_{GS} is the charge contained in this gate current pulse (7.2.1.1). From this charge value and the acceptable value of gate supply voltage increase, the designer can select the appropriate value of a gate decoupling capacitor. The nonrepetitive peak gate current is the gate impulse rating. High levels of gate current only occur during the initial part of fast-rising impulses. The specified gate peak current is applied to the gate and

adjacent terminal and uses a short impulse, such as a 1/2 or a 2/10. The designer should check that this rating is not exceeded if an unusual circuit configuration is used or very fast *di/dt* impulses occur.

7.3.3.5 Gate-to-adjacent terminal peak off-state voltage—V_{GDM}

This parameter is the equivalent to the main terminal V_{DRM} value for gated devices with a gate-blocking characteristic. As the maximum stress will be the same as V_{DRM}, the value and test conditions for V_{GDM} should be the same as V_{DRM} (7.3.2.2).

Annex A

(informative)

Example designs

A.1 Introduction

The designer wants a protection circuit solution that works, is durable, is efficient, and complies with the relevant standards. Standards formulate approaches and criteria. In some cases, the criteria may completely define the protector's parameters. As a result, products are likely to be available that comply with the performance standard's values, which eases the design task. In other cases, the criteria is general (e.g., shall continue to work after a test). In such cases, the designer also needs to know the protected circuit requirements to formulate the protection circuit parameters. Knowing these requirements, the designer would attempt a design using (standard) components that are available. If this was unsuccessful, then this might drive a change in the protection requirements to enable a standard component to be used or a request to component manufacturers for a special part. The following examples illustrate the three possible thyristor SPD situations: set by standard(s) alone, set by standard(s) and equipment withstand levels satisfied with available parts or special parts.

A.1.1 Two-point and multipoint protection

A single thyristor SPD, ThA, will limit the voltage across the conductors 1 and 2 that it is connected between (Figure A.1). Interconductor, two-point protection is commonly used for insulation protection of the subscriber line conductors and for limiting the overvoltage on equipment which has an isolation barrier at its interface to the line, e.g., modems with transformer or opto isolation. A symmetrical bidirectional SPD will limit the maximum positive and negative overvoltage levels to the same magnitude value (e.g., ±265 V). An asymmetrical bidirectional SPD will limit the maximum positive and negative overvoltage levels to different magnitude values (e.g., +190 V and –265 V). A unidirectional forward-conducting SPD will limit the maximum positive overvoltage to a diode forward conduction voltage and the negative overvoltage to the thyristor-limiting voltage (e.g., +2 V and –72 V).

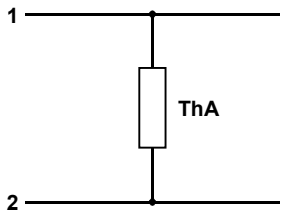

Figure A.1—Two-point parallel (shunt) connected protector

The most common form of multipoint protection is three-point protection, the three points being the two line conductors (1, 2) and the ground (Figure A.2). The simplest form uses two protectors (ThB and ThC), one from each conductor to the ground; so this is really two two-point protectors with a common point of ground. Relative to the ground, the limiting voltages on the conductors will be the same as discussed for the two-point protector.

The interconductor limiting voltage depends on whether the conductor overvoltages are common mode or differential mode (also referred to as longitudinal and metallic modes). Under common-mode conditions, the maximum interconductor voltage will occur when one protector (ThB or ThC) switches into a low-voltage,

on-state condition before the other. The maximum interconductor voltage will then be nearly the same as the maximum conductor to ground voltage. Under differential-mode conditions, protectors ThB and ThC are series connected across the two conductors. Thus, the maximum interconductor voltage could be the sum of the protectors $V_{(BO)}$ values, e.g., if the protectors were both ±300 V, the maximum interconductor voltage could be ±600 V. In many systems, higher interconductor voltages would not be a problem because the normal system interconductor voltages are higher than the conductor-to-ground voltages. In practice, perfectly balanced differential overvoltages are rare. Mixtures of common-mode and differential-mode overvoltages are produced by upstream protector operation and the transformer action in EMC filter chokes.

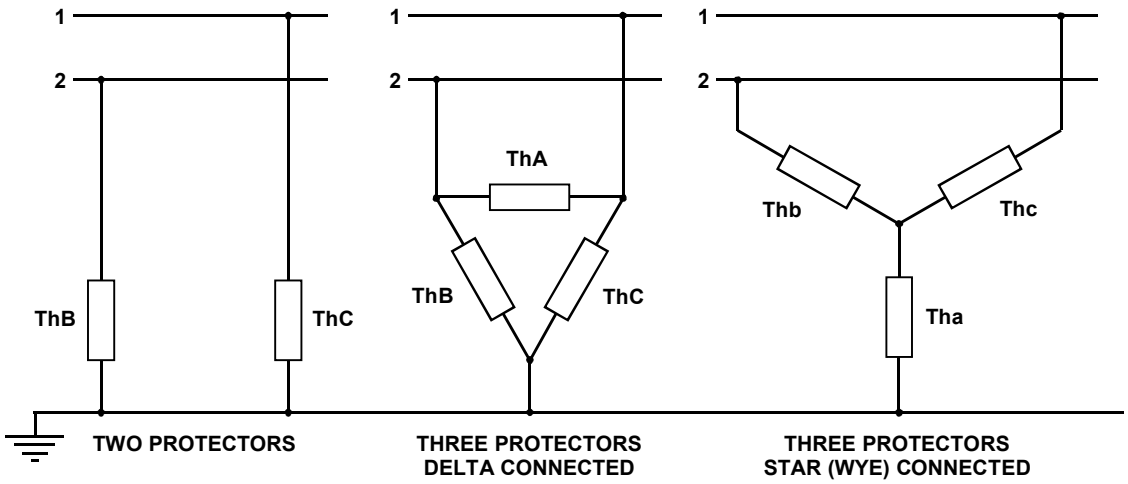

Figure A.2—Three examples of three-point protection

When it is desirable to lower the maximum interconductor voltage, an additional protector ThA can be used to form a delta connection (Figure A.2). If the $V_{(BO)}$ value of the protector ThA is less than the individual values of the other two protectors, then it is possible to have double the current flow in them. Under common- mode overvoltage conditions, if protector ThB switches on first, it places protector ThA in parallel with protector ThC. If protector ThA then switches on, it inhibits ThC conduction and diverts the conductor 1 current into ThB. Protector ThB then has the combined current of conductors 1 and 2, twice what might have been expected, which doubles the required current rating.

Similarly, if the three protectors are arranged in a star or Wye connection, protector Tha will always conduct the sum of the two line currents, e.g., for a 50-amp conductor impulse current, protector Tha would need a 100-amp rating. As the protectors are in series between any two protection points, the protector voltages will be half the values of the delta connection, e.g., if protectors with a $V_{(BO)}$ of ±300 V are used in the delta, ±150 V protectors would be needed in the star. Generally, protector Tha is designed to switch on before Thb and Thc which then causes the conductors to be pulled towards ground potential, increasing the conductor currents and causing Thb and Thc to switch on faster. A delta connection, having protectors with a $V_{(BO)}$ of ±300 V, could develop an maximum interconductor voltage of ±300 V during protector switching. In the case of the star connection, the maximum voltage is reduced to ±150 V.

The delta and star discussion assumes symmetrical bidirectional protectors. Asymmetrical or unidirectional protectors can also be used. In either case, this will result in different interconductor voltage waveforms and protector current levels. Series components in the conductor feeds may also cause different circuit operation.

A bridge circuit connection gives equal and symmetrical $V_{(BO)}$ voltages on any terminal pair (Figure A.3). During protector switching, the interconductor voltage is minimal. This configuration uses three components in series between any two protection points. As a result, the bridge connection has lower terminal capacitance than the other three-point circuits discussed. A lower inherent capacitance of the bridge

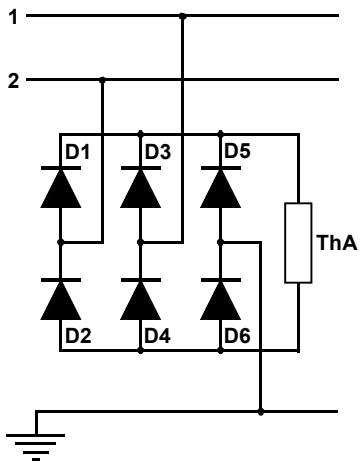

Figure A.3—Three-point protector using a single protector and bridge diodes

configuration compared with the configurations of Figure A.3 is useful for wide bandwidth systems. For a common mode positive polarity overvoltage, diode D1, D3 currents will be conducted through protector ThA and will return to ground via diode D6. When protector ThA switches, it will bring both conductors toward ground by pulling current through diodes D1 and D3 and returning it to ground via diode D6. The bridge will ensure the protector ThA only be surged in one polarity, and ThA can be a unidirectional protector. Combined conductor current ratings are needed for ThA and the ground return diodes D5 and D6. By adding further two diode strings, this protection scheme can be extended to protect a large number of terminals.

A.2 Primary protection application

This example illustrates the considerations in selecting thyristor SPDs for use in telephone primary surge protector units that are intended for controlled temperature environment applications.

A.2.1 Telephone system parameters

The following describes the telephone system parameters used in this example. The battery supply voltage is a maximum of 52-volt dc, and the maximum line conductor current is 260 mA. Voice, signaling, and data transmission frequencies are not greater than 1 MHz. The ringing signal voltage, when combined with battery bias, is a peak voltage of 195 V. AC 60-Hertz induction from joint power use of poles has peak values up to 10 V. Automated test systems are employed to alert maintenance personnel if system insulation resistance falls below 1.25 MΩ at 50-volt dc. Most of the equipment attached to the telephone system is rated at, and is capable of withstanding peak voltages of, 1 kV, without damage or degradation. However, the telephone company has elected to follow industry standards and apply a significant safety factor to reduce damage to more sensitive attached equipment over which they have no control. Therefore, they have specified that protectors shall prevent peak voltages in excess of 400 V from reaching protected equipment.

A.2.1.1 Transmission parameters

A.2.1.1.1 Off-state current—I_D

The off-state current will be measured as part of the system's leakage current and will influence the insulation resistance value. The maximum value of protector I_D is calculated from the minimum value of protector insulation resistance and the test voltage (±50 V) that is used. For the protectors only, PEG-7

requires no less than 10 MΩ (maximum I_D = ±5 μA), and Bellcore GR-974-CORE [B1] requires no less than 100 MΩ (I_D = ±0.5 μA). Users should apply which ever of these requirements fits their application.

Inasmuch as I_D increases with temperature, the user should specify thyristor protectors that have the required maximum I_D value at the worst-case (maximum) application temperature. In controlled environments, this is generally considered to be 50 °C (Bellcore TR-NWT-000063 [B5]). If the user is considering the application of these protectors to uncontrolled environments, such as non-air-conditioned huts or similar locations, then 65 °C is considered to be the appropriate maximum temperature.

A.2.1.1.2 Repetitive peak off-state voltage, V_{DRM} and breakdown voltage, $V_{(BR)}$

These parameters are used to ensure that the thyristor protector will not excessively clip the telephone ringing signal or cause unwanted ring trip occurrences. To ensure this, Bellcore has determined that taking into account dc powering voltage, ringing voltage, and allowable induced ac voltage, the protector should not conduct more than ±20 mA, when ±265 V is applied via a 1-kΩ resistor. Systems not conforming to the Bellcore standard may require higher or lower voltages.

The protector can be specified either for a low-current V_{DRM} condition or for a $V_{(BR)}$ measured at 20 mA. Figure A.4 shows the two different approaches. A protector specified for a 265-volt V_{DRM} at 10 μA will pass the Bellcore requirement because it will conduct only microamperes of current when the 265-volt test voltage is applied (dotted characteristic). A protector specified for a minimum 245-volt $V_{(BR)}$ at 20 mA will just meet the Bellcore requirement because it will conduct 20 mA when the 265-volt test voltage is applied (solid characteristic). Under this condition, the 20-volt drop caused by the 20-mA current in the 1-kΩ resistor reduces the 265-volt test voltage to 245 V on the protector.

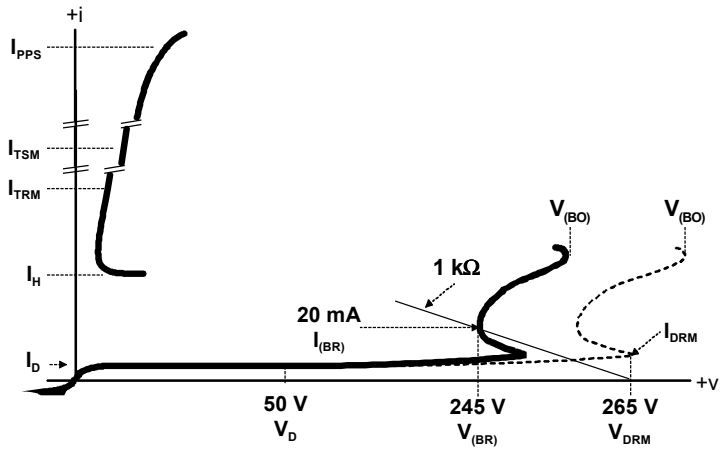

Figure A.4—Use of $V_{(BR)}$ or V_{DRM} for a 265-volt ring condition

A.2.1.1.3 Holding current—I_H

The holding current is the current at which the thyristor SPD switches from the on-state condition to the off-state condition. For the application, the holding current needs to be greater than the available short circuit current from the central office battery so that the thyristor device will turn off after switching into the on-state condition. In this example, the holding current should be greater than 260 mA. Holding current varies inversely with temperature. Therefore, the holding current should be specified at the highest expected temperature of the application, which is 50 °C.

The protector designer also needs to take into account the holding current reduction caused by residual temperature rise of the thyristor device after an impulse and temperature rise caused by the follow-on dc

power dissipation. Although temporary, this temperature rise can increase the amount of time that it takes for the thyristor to turn off after the surge has decayed.

A.2.1.1.4 Off-state capacitance—C_O

The capacitance value is useful to ensure that the thyristor protector unit will not load the telephone voice frequency or data signals. Bellcore has determined that line unbalance should not exceed 200 pF to avoid signal attenuation at frequencies up to 1 MHz. Compliance with this requirement is assured by setting the individual protector maximum capacitance (i.e., no dc bias voltage applied) to be no greater than 200 pF with a standard 1-volt rms signal applied (see Figure 15). If higher frequency signals are to be employed, a lower capacitance under the appropriate signal conditions may be required.

A.2.1.2 Protection

A.2.1.2.1 Breakover voltage—$V_{(BO)}$

The breakover voltage value should be selected to be low enough to be below the voltage that would damage the most sensitive component directly connected to the telephone lines. As indicated in the introductory paragraphs, Bellcore has determined that the 400-volt level should not be exceeded. Since the breakover voltage of the thyristor protector unit varies directly with temperature, the parameter should be specified at the highest temperature for the application, which is 50 °C in this case. Therefore, for this application, the $V_{(BO)}$ should be 400 V maximum at 50 °C.

A.2.1.3 Durability

A.2.1.3.1 Nonrepetitive peak pulse current—I_{PPS}

This parameter tells the user how much surge current the thyristor protector unit should be able to conduct without being damaged or destroyed. For this application, the protector unit is employed with hundreds or thousands of other protectors, on high pair-count telephone cables. Surges tend to be coupled and shared between many of the lines in a given cable. It has been shown that for urban and suburban high pair-count applications, the number of surges exceeding 100 A 10/1000 μs is vanishingly small. Therefore for this application, the I_{PPS} rating for satisfactory service life is 100 A 10/1000 μs. Since I_{PPS} can vary with temperature, it should be specified across the expected temperature range, which is 0 to 50 °C in this example.

A.2.1.3.2 Nonrepetitive peak on-state current—I_{TSM}

For reliable, long-life performance, it has been determined that protectors on telephone systems need to be able to survive at least 60 applications of 1 A rms 60 Hz for 1 second each, and at least 5 applications of 10 A rms 60 Hz for 1 second each. This test is done with a 600-volt rms voltage source to ensure protector breakover. These current values constitute the I_{TSM} of the thyristor surge protector and are applicable across the 0 to 50 °C temperature range for this application.

A.2.1.3.3 Repetitive peak on-state current—I_{TRM}

For reliable, long-life performance, it has also been determined that protectors on telephone systems need to survive very long duration applications of 0.5 A rms 60 Hz. Some protectors may be equipped with current-limiting or diverting devices that prevent overheating by limiting the duration of the current through the thyristor. The thyristor manufacturer should be consulted to determine if the device has an I_{TRM} rating sufficient to handle this current level. Table A.1 summarizes the device parameters for this example.

Table A.1—Summary of primary thyristor SPD parameters

Parameter	Rating or value for this application example
Transmission	
Off-state current, I_D	±0.5 μA maximum, V_D = ±50 V, 50 °C
Repetitive peak off-state voltage, V_{DRM} OR Breakdown voltage, $V_{(BR)}$	±265 V, I_{DRM} < ±10 μA, 0 < T_A < 50 °C ±245 V minimum, $I_{(BR)}$ = ±20 mA, 0 < T_A < 50 °C
Holding current, I_H	±260 mA minimum, T_A = 50 °C
Off-state capacitance, C_O	200 pF max. @ 1 V rms, 1 MHz, 0 dc bias
Protection	
Breakover voltage, $V_{(BO)}$	±400 V maximum, ±100 A 10/1000 μs, 0 < T_A < 50 °C
Durability	
Nonrepetitive peak pulse current, I_{PPS}	±100 A 10/1000 μs, 0 < T_A < 50 °C
Nonrepetitive peak on-state current, I_{TSM}	1 A rms, 60 Hz, 1 s, 60 applications, 0 < T_A < 50 °C 10 A rms, 60 Hz, 1 s, 5 applications, 0 < T_A < 50 °C
Repetitive peak on-state current, I_{TRM}	0.5 A rms, 900 s

A.2.2 Secondary protection

Secondary protection is normally incorporated into the equipment being protected. Thus, secondary protection design is diverse because it is equipment specific, whereas primary protection has to be general purpose because it may interface with a wide range of equipment.

A.2.2.1 Two-point protection example

This type of protection is for equipment that does not have a ground return, such as many telephones and modems. The protection function limits overvoltages that occur between the pair of conductors that form the telephone line. The U.S. FCC Part 68 standard [B7] was written to set mandatory equipment standards that would prevent harm to the telephone network or its personnel. Apart from environmental cycling, all remaining tests are done at room temperature.

Environmental simulation contains the lightning impulse tests with two types of impulse—Type A and Type B. Type A impulses are high stress level with 10/160 and 10/560 wave shapes. The equipment can be obviously nonoperational after a type A impulse. Type B surges are a less stressful 10/700 wave shape. The equipment shall be operational after a Type B impulse. Table A.2 shows the test levels and configurations. As a minimum, the thyristor SPD must be rated for the Type B impulse of 25 A, 5/320. If it is required that the equipment is also operational after a Type A impulse, then the thyristor SPD rating should be 100 A, 10/560. Upstream three-point protection could convert common mode impulses into differential mode (A.2.2.3). If this is a possibility, then to survive the thyristor SPD rating should be increased to meet the listed Ring/Tip to Ground impulse conditions given in Table A.2.

The highest voltage ringer test is for the class B type ringer. Here the ringing simulator consists of a 56.5 V dc supply and a 150 V rms ac source, which results in a peak voltage of 268.6 V. A protector with a V_{DRM} value of 275 V would not cause ring clipping and allows the device to be used in a lower ambient temperature. The protector $V_{(BO)}$ value is set by the protected component voltage rating. Typically, $V_{(BO)}$ values between 350 V and 400 V are used.

To meet the on-hook impedance limitations, the dc resistance between tip and ring must be greater than 5 MΩ for voltages up to 100 V (20 μA maximum at 100 V) and 30 kΩ between 100 V and 200 V (6.7 mA maximum at 200 V). Provided that the I_{DRM} value is less than 20 μA, the V_{DRM} specification satisfies this requirement.

Table A.2—FCC Part 68 conditions

Test	Open-circuit peak voltage V	Open-circuit voltage front time µs	Open-circuit voltage decay time µs	Short-circuit peak current A	Short-circuit current front time µs	Short-circuit current decay time µs
Type A	±800 (tip to ring)	10 max.	560 min.	100	10 max.	560 min.
	±1500 (tip/ring to ground)	10 max.	160 min.	200	10 max.	160 min.
Type B	±1000 (tip to ring)	9 µs ±30 %	720 µs ±20 %	25	5 µs ±30 %	320 µs ±20 %
	±1500 (tip/ring to ground)	9 µs ±30 %	720 µs ±20 %	37.5	5 µs ±30 %	320 µs ±20 %

Experience shows that in modern telephone systems a thyristor SPD holding a current value of 150 mA at 25 °C ambient is adequate.

To provide ac protection, some form of series current-reducing element shall be used. This series overcurrent protector can be a fuse, fusible resistor, or positive temperature coefficient (PTC) resistor. A simple fuse can meet all ac protection requirements. However, such a fuse can fail during impulse testing. To avoid fuse failure, an impulse-resistant fuse or a series resistor with a standard fuse can be used. The series resistor solution has the added benefit of reducing the protectors required impulse current rating and preventing excessive conductor impulse currents through lack of primary/secondary protector coordination (A.2.2.3). The PTC resistor resistance change resulting from overcurrent operation does not cause significant line unbalance for two-terminal systems. It is a consideration for three-terminal systems in which the differential resistance between the PTC resistors in each conductor may cause unacceptable line unbalance.

Compliance to UL 1459 product safety 50A section [B11] verifies that reasonable measures have been taken against fires caused by power line cross. UL 1459 is concerned with user and wiring safety. During and after testing, the equipment and its wiring feed shall not represent a hazard. Three types of hazards are defined—fire risk, electric shock, and unacceptable overcurrent conditions on the telecommunication wiring. Equipment failure is acceptable, provided a hazard does not occur.

There are three classes of equipment. They are as follows:

— Type I equipment has an acceptable form of inbuilt current limiting that limits the current to below the maximum specified limits.

— Type II equipment is only for use on protected wiring systems.

— Type III equipment is all other equipment classes.

Three variations of wiring simulator are specified. The most convenient simulator to use is the fuse (similar to Figure A.11) because it provides a simple go-no-go indication at the end of the test. In some tests (L1, L5, and M1) for Type I and Type II equipment, the wiring simulator could fail. Type II equipment shall withstand the current resulting from the test circuit and the wiring simulator fuse. In the referenced tests, at the short circuit current level, the fuse will rupture before the end of the test time. Type III equipment shall interrupt (or reduce the current to a low level) before the wiring simulator fails. For this to happen, the equipment must interrupt before 33 ms at 40 A and 87 ms at 25 A.

Table A.3—UL 1459 conditions

Test type	Test #	Open-circuit ac voltage V rms	Short-circuit current A rms	Test time s	Comments
Differential mode Applied ring to tip	M1	600	40	1.5	
	M2	600	7	5	
	M3	600	<2.2	1800	Current level shall not operate equipment current interruptor
	M4	<200	<2.2	1800	Current and voltage levels shall not operate equipment protection
Common mode Applied symultaneously ring to ground tip to ground	L1	600	40	1.5	
	L2	600	7	5	
	L3	600	<2.2	1800	Current level shall not operate equipment current interruptor
	L4	<200	<2.2	1800	Current and voltage levels shall not operate equipment protection
	L5	120	25	1800	

Longitudinal tests, L1 through L5, are only required if the equipment has its own ground elements (protectors). (See A.2.2.2.4 for this type of protection design.) Both tip and ring are simultaneously tested using separate current determining resistors. Metallic tests, M1 through to M4, have the tip or ring terminal grounded and the voltage is applied to ungrounded terminal. See A.2.2.2.4 for the formulation of the overcurrent protector specification and its coordination with the thyristor SPD ratings

(NOTE—Standards UL 1950 Third Edition [B6] and CAN/CSA-C22.2 No. 950-95 [B6] also incorporate the above tests).

Figure A.5 shows a typical protection circuit with the main thyristor SPD parameters specified.

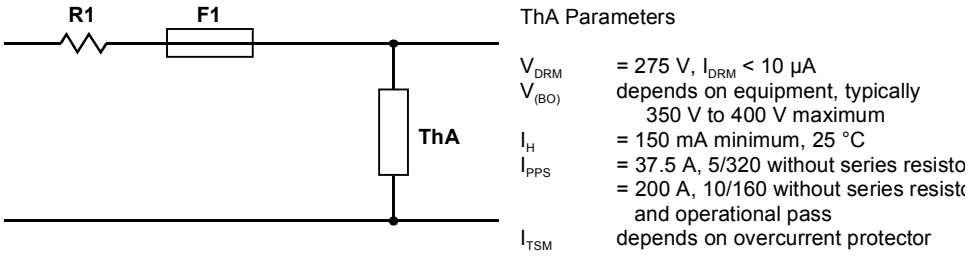

Figure A.5—Example Part 68 protection circuit

A.2.2.2 Three-point protection examples

A.2.2.2.1 Exchange subscriber line interface circuit (SLIC)

The telephone exchange interface to the line provides a function called BORSCHT, which stands for battery feed, overvoltage protection, ringing, signaling, coding, hybrid, and testing. The parts of this that influence the overvoltage protection design are shown in Figure A.6.

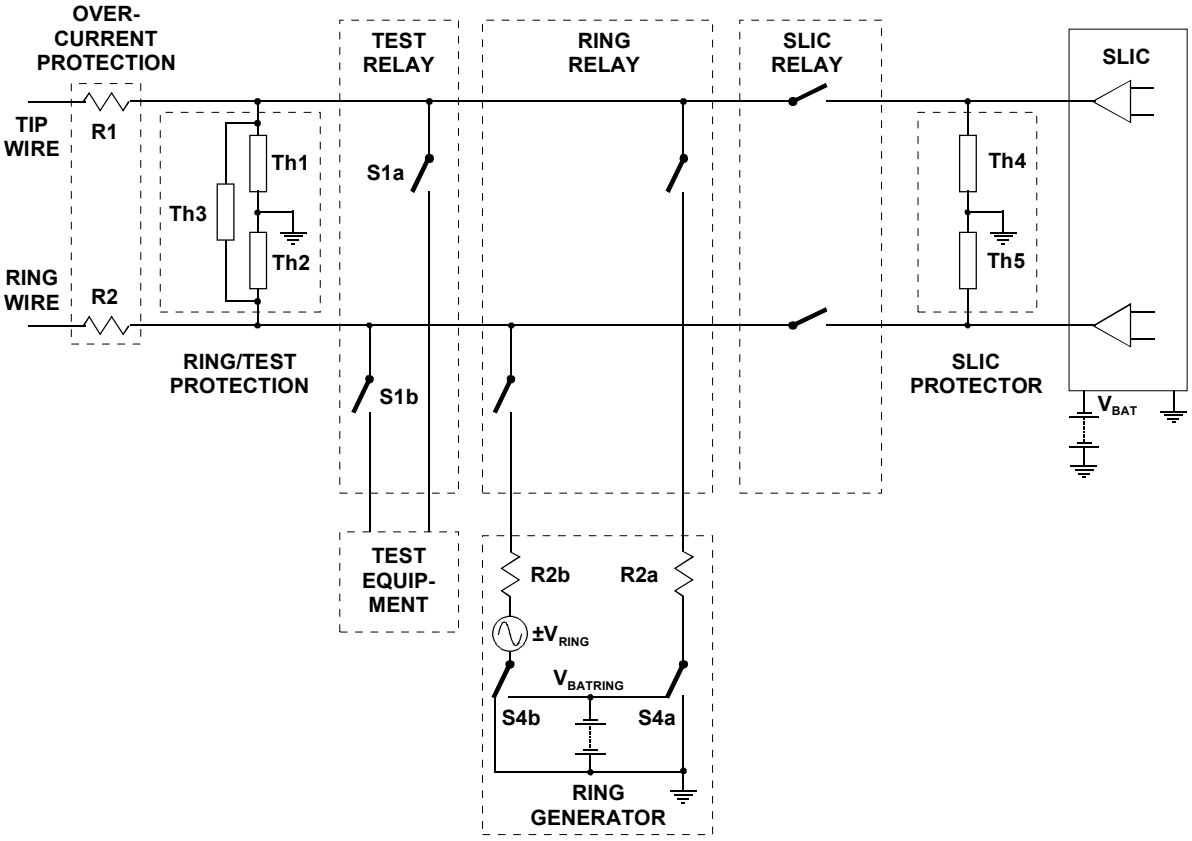

Figure A.6—Typical line interface circuit

Three relays (test, ring, and SLIC) control the application of the test, ring, and communication functions to the line. The three-point ring/test protector (nominally shown as a delta connection) protects the three relays, the test equipment, and the ring generator against overvoltages. Ahead of this is an overcurrent protector that operates to terminate any excessive ac power line contacted or induced currents. The SLIC is usually low voltage (< 100 V) and so has its own overvoltage protector (Th4 and Th5). When the SLIC relay closes, this parallels the two protectors and only the SLIC protector will operate as it has a lower limiting voltage.

A.2.2.2.2 Test and ring generator protection

It is usual for the ring generator to source the ac voltage to ring the telephone and a dc battery feed which is monitored. When current is detected from the dc feed, the telephone has been answered and the ring generator is disconnected and the SLIC connected to the line. The combination of ac and dc voltages may be applied in different ways depending on the local standards. It is common to apply both voltages to one line conductor and use the other conductor as the return path (switch S4 operated, Figure A.7). This configuration is termed *battery-backed ringing*. Some countries have the ac applied to one conductor and the dc applied to the other (switch S4 as shown; Figure A.7). This configuration is termed *ground-backed*

ringing. Another variant is to apply the ac to both conductors in a balanced manner. This configuration is termed *balanced ringing*.

At least 40-volt rms shall be applied to the handset to ring the telephone. To account for transmission losses, values of 70-volt rms are typically used. For these examples, a ring voltage range of 40-volt rms to 100-volt rms is considered. This represents peak ring voltage values, V_{RING}, of ±57 V to ±141 V. The dc battery feed voltage, $V_{BATRING}$, may nominally be –24 V or –48 V. For these examples, a battery feed voltage range of –20 V to –60 V is considered.

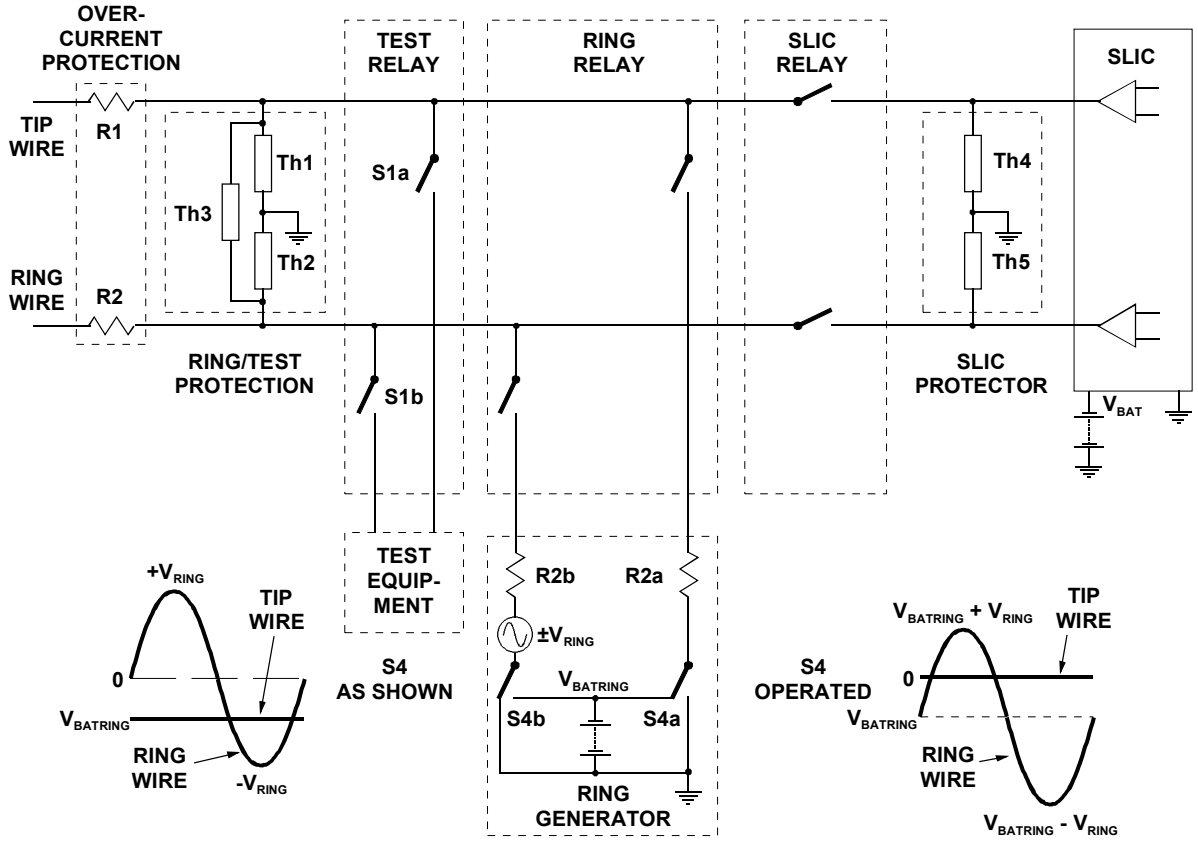

Figure A.7—Ring generator voltage levels

With reference to Figure A.7 (S4 as shown) and using the above ranges, the maximum open-circuit conductor voltage in the ground-backed ringing case is –60 V (tip) to ±141 V (ring). Protectors Th1 and Th2 should be specified with a V_{DRM} of ±141 V minimum to avoid ring clipping. Such protectors are likely to have $V_{(BO)}$ values in the ±180-volt region. The maximum interconductor voltage is +201 V and –121 V. If protector Th3 was used it would need a V_{DRM} of ±201 V, and this is likely to result in a $V_{(BO)}$ value of about ±265 V (lower than the 2x ± 180 = ±360 V level given by Th1 and Th2 in series). Typically, the ring generator circuit being protected would be mostly ground referenced with few, if any, susceptible components connected between the conductors. Hence, there is unlikely to be any benefit in including protector Th3 in this case.

The above assumes that the test equipment does not test at voltage levels above ±141 V. If it does test at higher levels, then the test equipment will set the protector V_{DRM} value.

With reference to Figure A.7 (S4 operated) and using the above ranges, the maximum open-circuit conductor voltage in the battery-backed ringing case is 0 V (tip) and –201 V to +121 V (ring). Protectors

Th1 and Th2 should be specified with a V_{DRM} of ±201 V minimum to avoid ring clipping. Such protectors are likely to have $V_{(BO)}$ values in the ±265-volt region. The maximum interconductor voltage is +201 V and –121 V. If protector Th3 was used, it would need a V_{DRM} of ±201 V, and this is likely to result in a $V_{(BO)}$ value of about ±265 V (lower than the 2x ± 265 = ±530 V level given by Th1 and Th2 in series. (See A.2.2.3.) In this case, there may be an advantage in using a delta- or star-connected protector.

Alternatively, Th1 and Th2 could be asymmetric bidirectional protectors with a V_{DRM} of –201 V and +121 V, giving likely $V_{(BO)}$ values of –265 V and +150 V. The maximum interconductor voltage would then be limited to ±415 V. Again, checks would have to be made to ensure that these voltage values would not restrict the operation of the test equipment. When the equipment is designed for battery-backed or ground-backed ringing, the protector voltages should cover both cases. The asymmetric protector values then become –201 V and +141 V V_{DRM}, giving -265 V and +180 V $V_{(BO)}$. Maximum interconductor voltage values become ±445 V.

The coordination of the overvoltage and overcurrent protectors is covered in A.2.2.2.4.

A.2.2.2.3 Solid-state relay protection

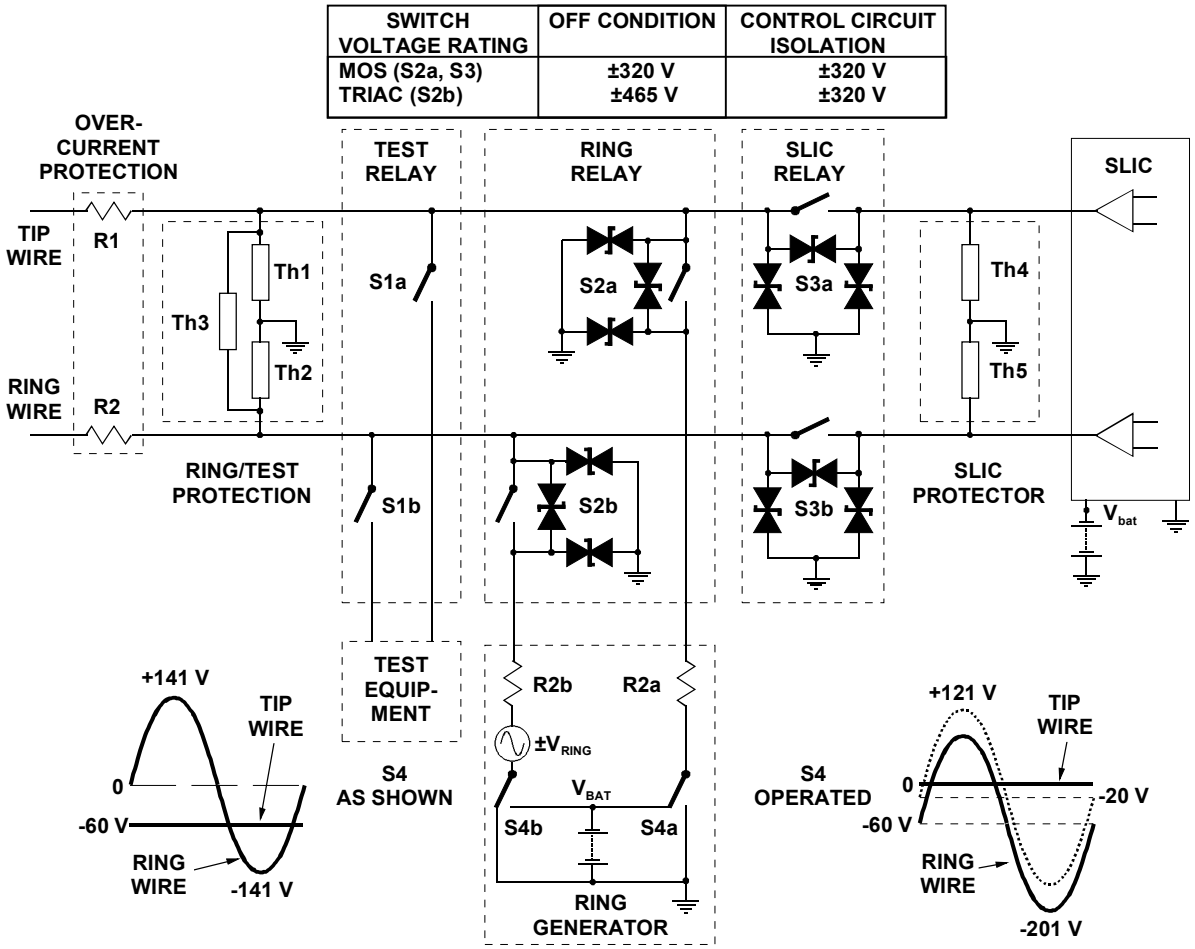

Figure A.8—Solid-state relay protection

Solid-state relays (SSRs) often use Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) and TRIAC-based switches to perform many of the normal electromechanical relay switch functions shown in Figure A.7. Being smaller, the SSR allows the design of higher function density line card printed circuit boards (PCBs). However, SSRs have lower withstand voltage than conventional relays. The table in Figure A.8 shows some typical values. The switches have two voltage limitations; one is switch breakdown in the off state (shown by a breakdown diode across the poles in Figure A.8) and the other is breakdown of the control line to the switch (shown by the two breakdown diodes to ground in Figure A.8). These breakdown levels change with temperature, but at the normal rate for semiconductor devices. Thus the thyristor SPD protection voltage is likely to track the change in SSR voltage withstand, allowing the initial protection design to be at 25 °C only. In the on-state condition, after a certain current level the MOSFET switches go into a current-limited mode and the voltage across them will rise to high levels. The resultant dissipation will be low for impulse conditions, but could rise to destructive values for low current ac power cross conditions. Thermal shutdown protection, to turn the switch off, is often incorporated in the switch array to prevent long-term overdissipation.

The MOSFET switches are rated at ±320 V to ground and across the switch in the off state. The non-line conductor end of switches S2a, S3a, and S3b could be at 0 or –60 V depending on the SLIC condition and the ringing configuration. Relative to ground, the line end of these switches should be limited to –320 V and +320 – 60 = +260 V. In the off state, the ±465 V TRIAC limit gives +465 – 201 = +264 V and –465 + 141 V = –324 V. These are higher than the MOSFET switch levels and so the maximum voltage applied to the SSR should not exceed +260 V and –320 V. These values are for worse-case conditions such as a fast rising impulse. Assuming that $V_{(BO)}$ rises by 15% under fast-rising impulse and long-term ac power induction conditions, the 50/60 Hz single cycle $V_{(BO)}$ values become +226 and –278 V. Previously, the protector V_{DRM} values were determined as +141 V and –201 V. (See A.2.2.2.2.) It would be difficult to meet this requirement with a symmetrical bidirectional protector as the V_{DRM} and $V_{(BO)}$ values would be very close, i.e., ±201 V and ±226 V, a 12% difference. Typically, the minimum achievable difference between V_{DRM} and $V_{(BO)}$ is 20% to 35% depending on voltage. An asymmetrical protector would be suited for this application because it would have V_{DRM} and $V_{(BO)}$ values of +141 V/–201 V and +226 V/–278 V, respectively (e.g., 60% and 38% differences).

As all switches are referenced to ground, there is no need for the inclusion of protector Th3. If necessary, to allow an extra 20-volt excursion in the positive test voltage level, the protector positive V_{DRM} could be increased to +160 V. The voltage levels on the tip conductor protector, Th1, could be further reduced because the ringing voltage is much less on this conductor (possibly only 50% of the open-circuit value). The minimum Th1 protector voltage may then be set by the test voltage levels used. Due to the wide range of values chosen, this application would be best served by custom protectors targeted to the levels of the specific equipment.

A.2.2.2.4 LSSGR subscriber line interface circuit protection

In Figure A.6, the SLIC output stages are powered between ground and the negative battery supply, V_{BAT}. The output stage protectors, Th4 and Th5, should limit overvoltages that go positive of ground and negative of the battery supply. Unidirectional protectors will do this because positive excursions are clipped to ground by the diode characteristic and large negative excursions are limited by the thyristor switching characteristic (see Figure 9).

Figure A.9 shows fixed voltage and gate-controlled Th4/5 protector options. In both cases, positive impulse currents are diverted to ground by a forward-conducting diode. The fixed voltage protector limits the negative impulse voltage to $V_{(BO)}$. In many designs, a fixed protection voltage level is adequate. When the SLIC supply voltage may vary over a large range or the SLIC requires minimal voltage stress, a gate-controlled (programmable) thyristor SPD is often used. As the gate is referenced to the SLIC V_{BAT} supply, the protection voltage tracks the value of V_{BAT}. A gate buffer transistor is often used to reduce the current levels injected into the V_{BAT} supply under power contact and induction conditions.

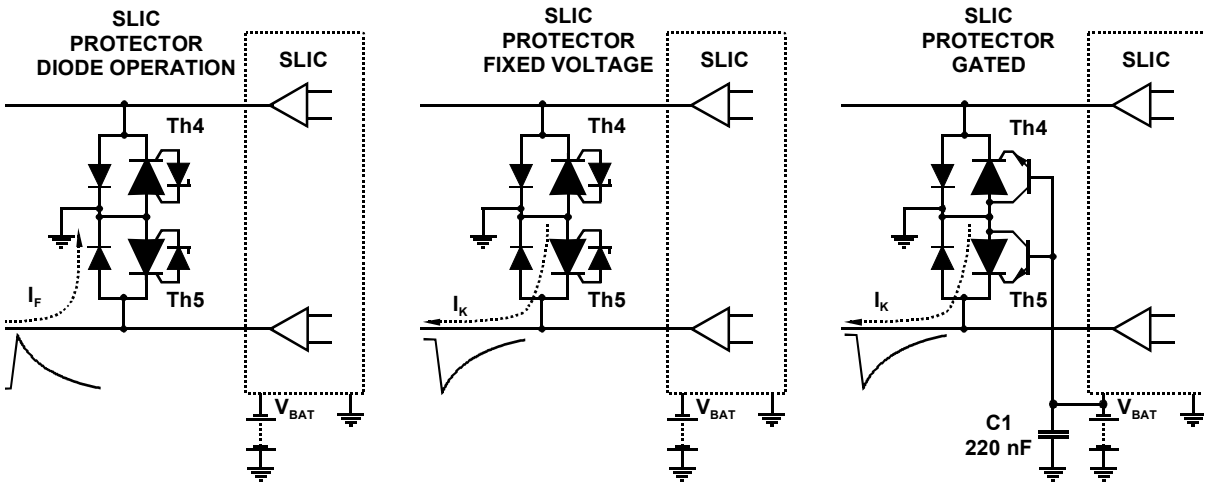

Figure A.9—Unidirectional fixed voltage and gate-controlled protectors

Some SLIC designs remove the need for relays and a ring generator by having the SLIC produce the ringing voltage. To generate sufficient ringing voltage, these SLICs are often powered by similar positive and negative supply voltages. Such designs require bidirectional protection. Figure A.10 shows one protection configuration. The diode bridge, D1, D2, D3 and D4, applies positive conductor voltages to the N-gate protector Th4 and negative conductor voltages to the P-gate protector Th5. When the applied voltage exceeds the battery voltage that the gate is referenced to, the protector switches into the on-state. The series gate diodes prevent shorting the battery supply to ground when the protector switches on.

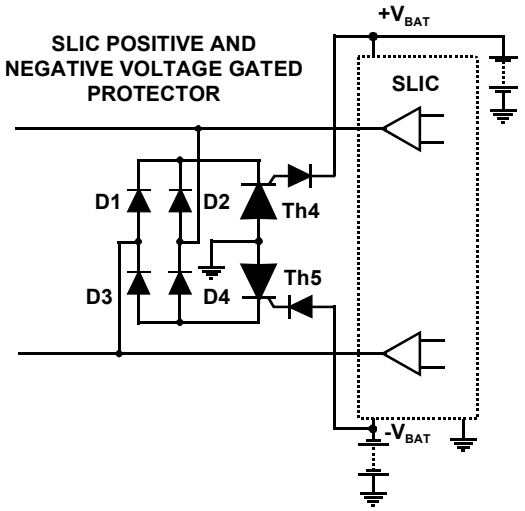

Figure A.10—Positive and negative gate-controlled protection

This example takes a specified thyristor SPD and creates an LSSGR-compliant [local access transport area (LATA) switching systems generic requirements] design that does not exceed the device ratings. The rated 10/1000 current for the chosen device was 30 A. For first level surge survival, the minimum value of series resistance for this application is 25 Ω (R1 and R2 in Figure A.6). This gives a peak impulse current of 29 A 10/1000 current in the device during first-level testing. (A higher rated protector could use a lower resistor value e.g a 50 A 10/1000 device would use 10 Ω) For second-level surge testing, survival the resistor value must be increased to 40 Ω. This design will be for second-level surge survival and so will use a series resistor value of 40 Ω. The specified ratings for each protector are given in Table A.4.

Table A.4—Protector parameters

Rating	Symbol	Value	Unit
Nonrepetitive peak on-state pulse current	I_{PPS}		A
10/1000 μs		30	
1.2/50 μs		100	
2/10 μs		120	
Nonrepetitive peak on-state current, 60 Hz	I_{TSM}		A
0.1 s		11	
1 s		4.5	
5 s		2.4	
300 s		0.95	
900 s		0.93	

GR-1089-CORE [B3], "1089," covers electromagnetic compatibility and electrical safety generic criteria for U.S. network telecommunication equipment. It is a module in Volume 3 of LSSGR (FR-NWT-000064). In 1089, surge and power fault immunity tests are done at two levels. After first-level testing, the equipment shall not be damaged and shall continue to operate correctly. Under second-level testing, the equipment shall not become a safety hazard. The equipment is permitted to fail as a result of second-level testing. When the equipment is to be located on customer premises, second-level testing includes a wiring simulator test, which requires the equipment to reduce the power fault current below certain values.

The following clauses reference the 1089 section and calculate the protector stress levels. The values of protector current are calculated from the open circuit generator voltage divided by the sum of the total circuit resistance. The total circuit resistance is the sum of the generator fictive source resistance and the device series resistor value. Most generators have multiple outputs, and each output connects to an individual line conductor. For those generators that have a single output, each conductor will have an effective generator fictive source resistance of n times the generator fictive source resistance, where n is the number of conductors simultaneously tested.

A.2.2.2.4.1 GR-1089-CORE section 4.5.7—First-level surge testing

The two most significant test wave shapes in this section are the high energy 10/1000 and the high current 2/10. As shown in Table A.5, the peak currents for these impulses are 2 × 20 A and 2 × 56 A respectively. (The 2 × 20 A designation means that simultaneous impulses occur on both the ring and tip conductors. The tip conductor current is 20 A, and the ring conductor current is 20 A.) The protector shall survive the 2 × 20 A 10/1000 impulse, and the device will do this because its rating is 2 × 30 A. When both conductors are surged simultaneously, the ground return current will be 40 A; again, the device will survive this because its rating for this condition is 60 A. Similarly the device will survive the 2 × 56 A 2/10 because its rating is 2 × 120 A.

Table A.5—First-level surge currents

Wave shape	Open-circuit voltage V	Short-circuit current A	Generator fictive source resistance Ω	Total circuit resistance Ω	I_T A
2/10	2500	500	5	45	2 × 56
1.2/50, 8/20	2500	360	4 + 3	47	2 × 53
10/360	1000	100	10	50	2 × 20

Table A.5—First-level surge currents *(continued)*

Wave shape	Open-circuit voltage V	Short-circuit current A	Generator fictive source resistance Ω	Total circuit resistance Ω	I_T A
10/1000	600	100	6	46	2 × 13
10/1000	1000	100	10	50	2 × 20

The highest protection voltage will be for the 56-amp 2/10 wave shape. Under this condition, the average rate of current rise will be 56/2 = 28 A/μs. The value of diode and thyristor voltage under this condition needs to be specified in the device electrical characteristics.

Compared with TR-NWT-001089 [B4], GR-1089-CORE [B2] adds the alternative of using the IEC 61000-4-5 1.2/50-8/20 combination wave generator for the 2/10 test. This generator usually has a single output and a fictive resistance of 2 Ω. The 2/10 generator has a fictive output resistance of 5 Ω, (2500/500), and GR-1089-CORE compensates for this by adding an extra 3 Ω in the output of the 1.2/50-8/20 generator. In practice, the extra 3 Ω causes the prospective short-circuit current wave shape to be similar to the 1.2/50 open-circuit voltage wave shape. The device will survive the 2 × 53 A 1.2/50 because its rating is 2 × 100 A.

A.2.2.2.4.2 GR-1089-CORE section 4.5.8—Second-level surge testing

This is a 2/10 wave shape test. As shown in Table A.6, the peak current for this impulse is 2 × 100 A. The device will survive the 2 × 100 A 2/10 impulse because its rating is 2 × 120 A.

Table A.6—Second-level surge currents

Wave shape	Open-circuit voltage V	Short-circuit current A	Generator fictive source resistance Ω	Total circuit resistance Ω	I_T A
2/10	5000	500	10	50	2 × 100
1.2/50, 8/20	5000	420	4 + 8/conductor	52	2 × 96

Under this condition, the average rate of current rise will be 100/2 = 50 A/μs. The value of diode and thyristor voltage under this condition needs to be specified in the electrical characteristics.

The 2/10 generator has a fictive output resistance 10 Ω, (5000/500), and GR-1089-CORE matches the 1.2/50-8/20 generator to this by adding an extra 8 Ω in the output. In practice, the extra 8 Ω causes the prospective short-circuit current wave shape to be similar to the 1.2/50 open-circuit voltage wave shape. The device will survive the 2× 96 A 1.2/50 because its rating is 2 × 100 A.

A.2.2.2.4.3 GR-1089-CORE section 4.5.9—Intra-building surge testing

These tests use a 2/10 wave shape. As shown in Table A.7, the peak currents for this test are 2 × 27 A and 17 A. The device can survive both these levels because its rating is 2 × 120 A.

The 2/10 generator has fictive output resistances of 15 Ω and 8 Ω. GR-1089-CORE matches the 1.2/50-8/20 generator to this by adding the extra resistances of 12 Ω and 6 Ω in the output. In practice, this extra resistance causes the prospective short-circuit current wave shape to be similar to the 1.2/50 open-circuit voltage wave shape. The device will survive the 2 × 27 A 1.2/50 because its rating is 2 × 100 A.

Table A.7—Intra-building surge currents

Wave shape	Open-circuit voltage V	Short-circuit current A	Generator fictive source resistance Ω	Total circuit resistance Ω	I_T A
2/10	1500	100	15	55	2 × 27
	800	100	8	48	17
1.2/50, 8/20 (See text)	1500	94	4 + 12/conductor	56	2 × 27
	800	100	2 + 6	48	17

A.2.2.2.4.4 GR-1089-CORE section 4.5.12 —First-level power fault testing

The most significant tests are a long-duration (900 s) medium current test and a higher current tests of 60, one second power applications. As shown in Table A.8, the peak currents for these tests are 2 × 0.37 A and 2 × 1.3 A, respectively. The device will survive both of these conditions because its ratings are 2 × 0.93 A and 2 × 4.5 A for these time periods.

Table A.8—First-level power fault currents

AC duration s	Open-circuit rms voltage V	Short-circuit rms current A	Source resistance Ω	Total circuit resistance Ω	I_{TRMS} A	I_{TM} A
1	200	0.33	600	640	2 × 0.31	2 × 0.44
1	400	0.67	600	640	2 × 0.63	2 × 0.88
1	600	1	600	640	2 × 0.94	2 × 1.3
1	1000	1	1000	1040	2 × 0.96	2 × 1.3
900	50	0.33	150	190	2 × 0.26	2 × 0.37
900	100	0.17	590	630	2 × 0.16	2 × 0.22

A.2.2.2.4.5 GR-1089-CORE section 4.5.13—Second-level power fault testing

The two most significant tests are a long-duration (900 s) medium current test and a higher current 5-second test. As shown in Table A.9, the peak currents for these tests are 2 × 17 A and 2 × 7.7 A respectively. For the device to survive this test, the series overcurrent protection shall operate within 0.1 s and 0.5 s, respectively.

Table A.9—Second-level power fault currents

AC duration s	Open-circuit rms voltage V	Short-circuit rms current A	Source resistance Ω	Total circuit resistance Ω	I_{TRMS} A	I_{TM} A
5	600	60	10	50	2 × 12	2 × 17
5	600	7	86	126	2 × 4.8	2 × 6.8
900	120	25	5	45	2 × 2.7	2 × 3.8
900	277	25	11	51	2 × 5.4	2 × 7.7

Table A.9—Second-level power fault currents *(continued)*

AC duration s	Open-circuit rms voltage V	Short-circuit rms current A	Source resistance Ω	Total circuit resistance Ω	I_{TRMS} A	I_{TM} A
900	100	0.37	273	313	2×0.32	2×0.45
900	300	1.1	273	313	2×0.96	2×1.4
900	600	2.2	273	313	2×1.9	2×2.7

A.2.2.2.4.6 GR-1089-CORE section 4.5.15—Second-level power fault testing with wiring simulator

The purpose of this test is to ensure that the telephone cable does not become a hazard due to excessive current. A series fuse, type MDQ 1-6/10A, simulates the safe current levels of a telephone cable. If this fuse opens, the equipment fails the test. For the equipment to pass, the equipment series overcurrent element shall reduce the current to below the MDQ 1-6/10A fusing level to prevent the simulator operating. The ac test voltage can range from zero to 600 V, which gives a maximum conductor current of 10 A. Table A.10 shows the simulator fusing times for three current levels.

Table A.10—Second-level power fault currents with MDQ 1-6/10A fuse

AC duration s	Open-circuit rms voltage V	Short-circuit rms current A	Source resistance Ω	Total circuit resistance Ω	I_{TRMS} A	I_{TM} A	Time to open s
1000	100	5	20	60	1.7	2.4	—
1000	300	15	20	60	5.0	7.1	30
1000	600	30	20	60	10	14	0.7

For the equipment to pass this test, the device series current-limiting element must operate before the MDQ 1-6/10A fusing times shown in Table A.11.

Table A.11—Operating times of MDQ 1-6/10A fuse

Time to operate s	I_{RMS} A
0.2	17
0.5	12
1	9
5	7
10	6.8
1000	2.5

A.2.2.2.4.7 overcurrent protection

To meet Bellcore GR1089, the overcurrent protection shall be coordinated with the requirements of sections 4.5.7, 4.5.8, 4.5.9, 4.5.12, 4.5.13, 4.5.15 and the device. The overcurrent protection shall not fail in the first level tests of sections 4.5.7, 4.5.9, and 4.5.12. Recoverable overcurrent protectors (e.g., PTCs) may operate during first level testing, but normal equipment working shall be restored after the test has ended. The test current levels and their duration are shown in Figure A.11. First level tests have a high source resistance, and the current levels are not strongly dependent on the device series resistor value.

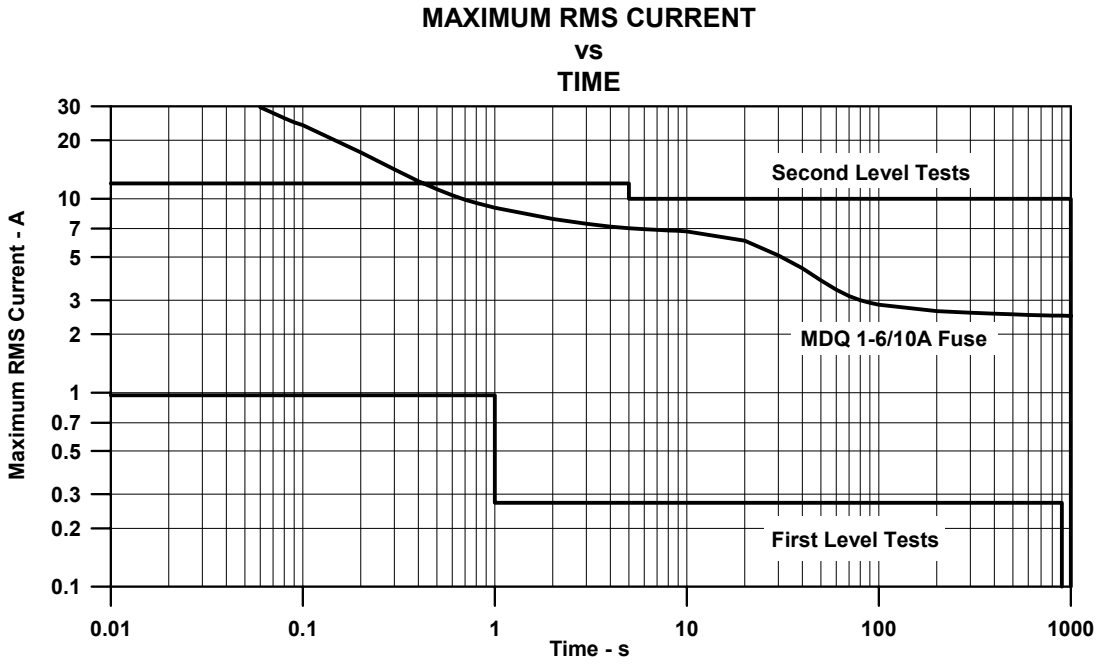

Figure A.11—1089 maximum test current level

Second-level tests have a low source resistance, and the current levels are dependent on the device series resistor value. The stepped line at the top of Figure A.11 is for the 40-ohm series resistor case. If the full current-time durations occur, the equipment will fail the wiring simulator test. The MDQ 1-6/10A fusing characteristic is also shown in Figure A.11. The device series overcurrent protection shall operate before the MDQ 1-6/10A fuses; so this represents another boundary condition in the selection of the overcurrent protector.

Figure A.12 summarizes these boundary conditions. The highest current levels that can flow are influenced by the device series resistance. After 0.4 s, the maximum current-time boundary becomes set by the MDQ 1-6/10A fusing characteristic. Fusible overcurrent protectors cannot operate at first-level current levels.

Figure A.12 also shows the device-rated current versus time. The overcurrent protector should not allow current-time durations greater than this; otherwise, the device may fail. If second-level failure is acceptable, then the overcurrent protector *shall* operate before the device package limit is reached.

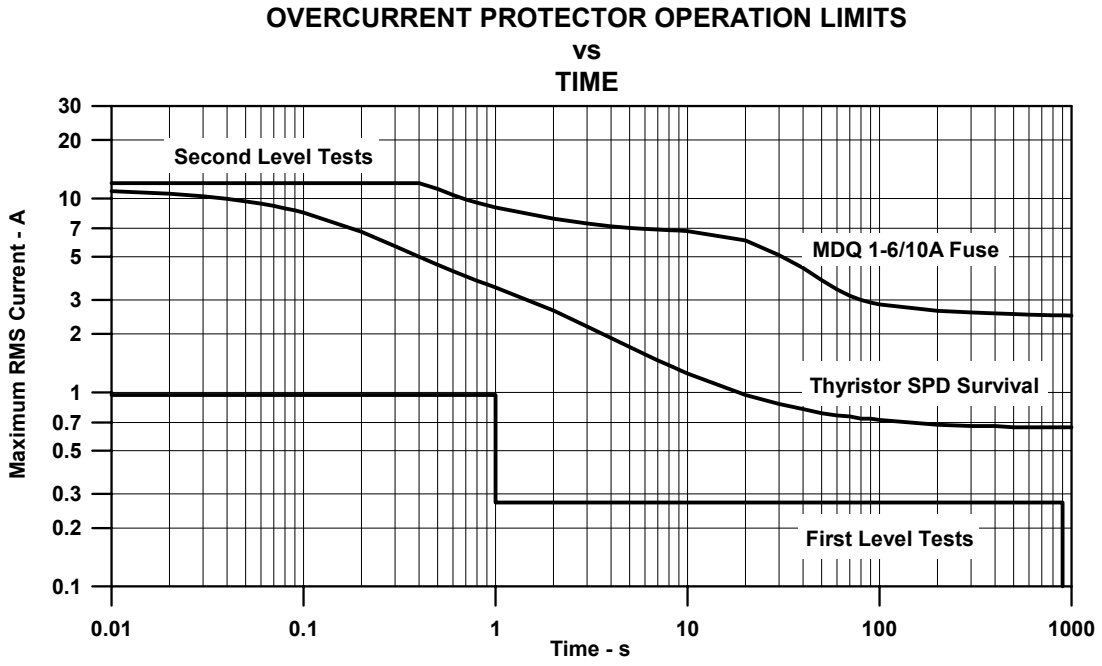

Figure A.12—Overcurrent protector requirements

A.2.2.3 Coordination of protection

A.2.2.3.1 Primary and secondary coordination

When a secondary thyristor SPD switches into a low-voltage state, it can prevent the upstream primary protector device from operating. Figure A.13 shows how this can happen. On its own, a primary thyristor SPD ThA diverts a peak impulse current of I_{AM} from a given impulse [Figure A.13(a)]. Figure A.13(b) connects a secondary thyristor SPD ThB downstream at distance l away from ThA. If any inductance and transit time effects are ignored, the two protectors can be considered as connected in parallel. As ThB typically has a lower breakover voltage than ThA does, a rising impulse will switch protector ThB into the on-state condition first. Once in a low-voltage, on-state condition, protector ThB inhibits the switching of protector ThA. Protector ThB then diverts a peak current of I_{BM}, which is the same as the original I_{AM} value. As the secondary protectors are usually lower in current value than are primary protectors, protector ThB may fail in diverting the impulse current that should have been carried by ThA. Further, ThB conduction causes high currents to be propagated beyond the primary interface, which may cause undesirable effects.

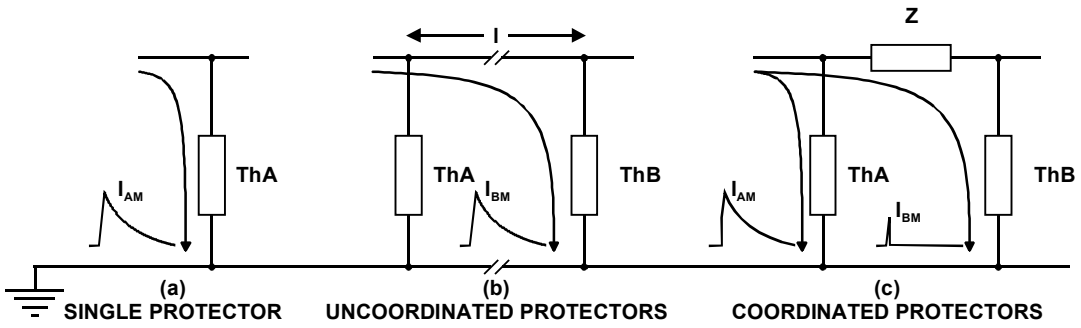

Figure A.13—Protector coordination by series element

The devices of this example can be coordinated by inserting a series impedance Z between the two protectors. This will not stop the early switch on of protector ThB, but the current flowing in the impedance will generate sufficient voltage to switch protector ThA. Once protector ThA is in the on-state condition, it will divert the remaining impulse current.

Attempts have been made to use wiring inductance, of conductor length l, to generate back-emf voltages to trigger ThA. Also, wiring transit times (time to travel distance $2l$) have been used (about 9 ns/m) to give protector ThA time to breakover before the reflected low voltage from ThB arrives back. Both of these methods fail for slow-rising impulses and ac. One method to ensure sufficient voltage to operate ThA is to use a series resistance. If the impulse current rating of ThB is I_B and the maximum breakover voltage of ThA is V_A, then the series resistor R should be greater than V_A/I_B.

The total impulse current is diverted by protector ThB at low levels of current up to the rated current of ThB. At current impulse levels above the rated current of ThB, protector ThB conducts for the short period before ThA switches. This example used a voltage-switching type primary protector (thyristor, GDT). The same design approach can be used for voltage-clamping type primary protectors. Some telephone companies ban the use of such techniques.

A.2.2.3.2 Coordination among secondary protective devices

Figure A.14 shows how the choice of interconductor $V_{(BO)}$ value is critical. Without the interconductor protector ThA (a), protectors ThB and ThC carry equal peak impulse currents, I_{2M} and I_{1M}. If protector ThB has a slightly lower value of breakover voltage than protector ThC does, protector ThB will switch on first. When protector ThA present [(b) and (c)], the on-state of protector ThB effectively connects protector ThA in parallel with protector ThC. If protector ThA has a lower breakover voltage than ThC (b) does, then it will switch on before ThC. This diverts the current, which should have been diverted by ThC into ThB. As a result, protector ThB diverts twice the expected current ($I_{1M} + I_{2M}$). By setting the protector ThA to have the higher $V_{(BO)}$ than either ThB or ThC (c), the conductor impulse currents are diverted by the appropriate protector.

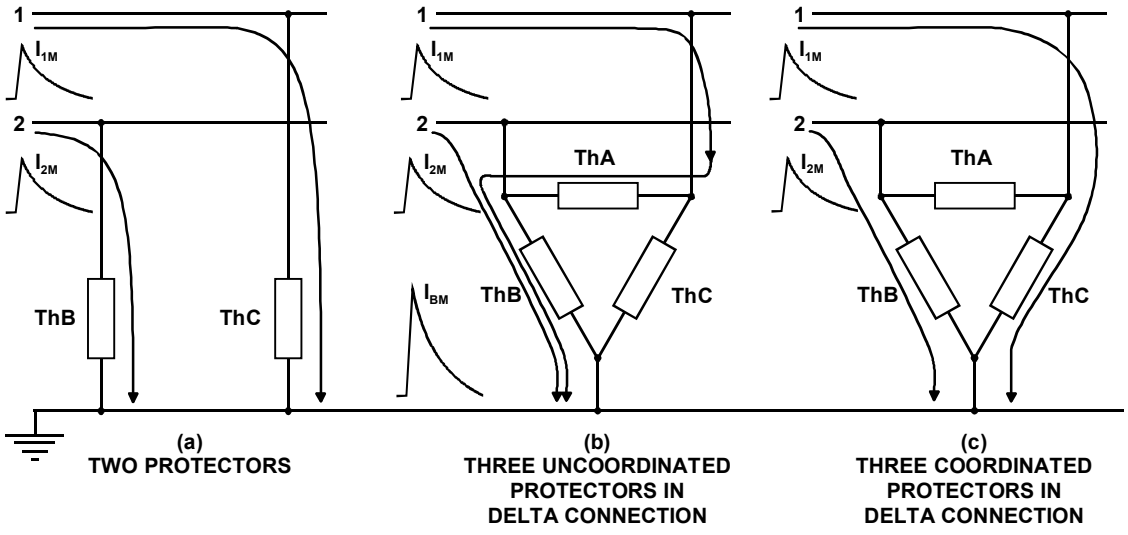

Figure A.14—Interconductor $V_{(BO)}$ value

A.2.2.3.3 Current triggered protectors

Current triggered protectors can give coordination with a smaller series resistance between the protectors than needed in Figure A.13. Figure A.15 shows the configuration. The protector ThA is formed by an N-gate

and a P-gate thyristor connected in antiparallel. The gates of the two thyristors are connected together. Resistor R is connected in series with the circuit conductors and between the protector ThA common adjacent terminals and the connected gates. Current flowing in the conductor will develop a voltage across resistor R. Normally, the circuit current would not develop sufficient voltage across the resistor to trigger the protector ThA. Under impulse conditions, protector ThB would switch on and divert current. In doing so, protector ThA would be triggered.

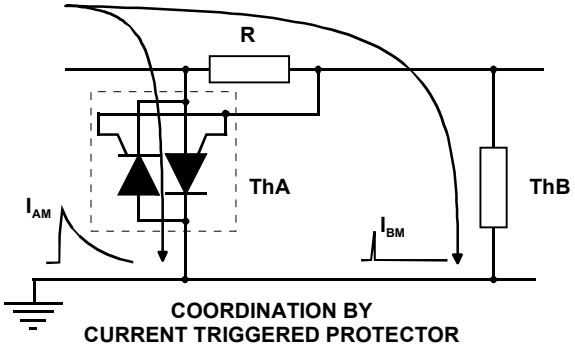

Figure A.15—Current triggered protector coordination

To protect when the protector ThB is not connected, protector ThA can also operate as a fixed voltage protector by the addition of the two breakdown diodes that connect the appropriate gates together. (See Figure A.16.)

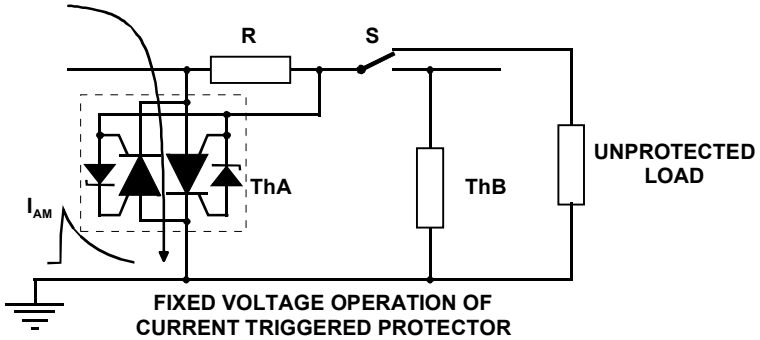

Figure A.16—Current triggered protector coordination

Annex B

(informative)

Comparison of dependability definitions

B.1 durability: The ability of an item to perform a required function under given conditions of use and maintenance, until a limiting state is reached.

NOTE—A limiting state of an item may be characterized by the end of useful life, unsuitability for any economic or technological reasons, or other relevant factors. IEV

B.2 reliability (performance): The ability of an item to perform a required function under given conditions for a given time interval.

NOTES

1—It is generally assumed that the item is in a state to perform this required function before the beginning of the time interval.

2—The term “reliability” is also used as a measure of reliability performance. IEV

B.3 reliability [$R(t_1, t_2)$]: The probability that an item can perform a required function under given conditions for a given time interval (t_1, t_2).

NOTES

1—It is generally assumed that the item is in a state to perform this required function before the beginning of the time interval.

2—The term “reliability” is also used to denote the reliability performance quantified by this probability. IEV

B.4 reliability (general): (1) The ability of an item to perform a required function under stated conditions for a stated period of time.

NOTE—The term “reliability” is also used as a reliability characteristic denoting a probability of success, or a success ratio. IEEE 100 [B8].

(2) The probability that a device will function without failure over a specified time period or amount of usage.

NOTES

1—This definition is commonly used in engineering applications. In any case where confusion may arise specify the definition being used.

2—The probability that the system will perform its function over the specified time should be equal to or greater than the reliability. IEEE 100 [B8].

Annex C

(informative)

SPD technology comparison

C.1 Voltage-limiting SPDs

The purpose of this annex is to describe the main features of the different SPD technologies. Voltage-limiting SPDs are shunt, non-linear elements that limit overvoltages that exceed a given rated voltage by providing a low impedance path to divert currents. This rated voltage is chosen to be the maximum peak system voltage in normal operation. At this rated voltage the conducted current of the SPD component should not interfere with normal system operation. The maximum voltage level developed across the SPD component during an overvoltage surge is equal to or less than the guaranteed voltage protection level of the component. (Figure C.1.)

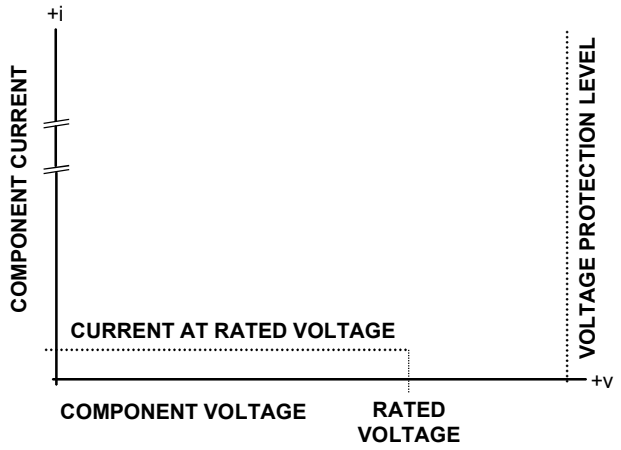

Figure C.1—SPD component-rated voltage and voltage protection level

Multiple components may be used to form assemblies. An increased voltage level may be achieved by connecting the components in series. The parallel component connection will increase the surge current capability of the assembly. However, care should be taken to assure current sharing between the parallel components.

Some technologies (e.g., metal oxide varistor) have voltage-current characteristics that are inherently symmetrical for positive and negative voltage polarities. Such devices are classified as symmetrical bidirectional. Devices having positive and negative voltage-current characteristics with the same basic shape, but with significantly different characteristic values, are classified as asymmetrical bidirectional.

Other technologies (e.g., PN semiconductor junctions) have voltage-current characteristics that are inherently different for positive and negative voltage polarities. Such devices are classified as unidirectional.

C.1.1 Voltage clamping type

These SPD components have a continuous voltage-current characteristic. Generally, this will mean that the protected (downstream) equipment will be exposed to a voltage above the rated level for most of the voltage

impulse duration. As a result, these SPD components will absorb substantial energy during the overvoltage. (Figure C.2 and Figure C.3.)

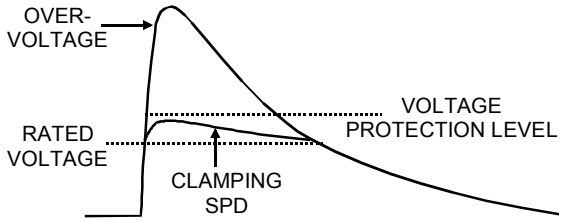

Figure C.2—Voltage limiting of clamping SPD

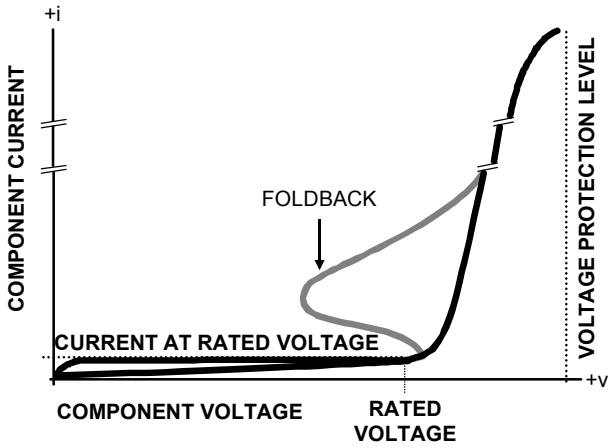

Figure C.3—Voltage-clamping SPD characteristics for different technologies

C.1.1.1 Metal oxide varistor

A metal oxide varistor (MOV) is a ceramic, non-linear resistor made from metal oxides. Over most of the voltage-limiting range, the MOV voltage increases non-linearly with increasing current. At the highest current levels, the material bulk resistance predominates, linearizing the characteristic.

MOV components are available with rated (reference) voltages of 5 V and greater. Under high-current impulse conditions, the MOV-limiting voltage can increase significantly. This can help in coordinating the operation of cascaded SPDs, but the downstream equipment may be exposed to high-voltage levels.

The MOV has a fast response time, making it suitable to limit rapidly rising transient voltages. It also has a high thermal capacity and can absorb high current impulses. Large numbers of rated impulses or a few excessive ones may degrade the MOV. This aging process needs to be comprehended to achieve the desired service life. On high-frequency systems, the relatively large capacitance of the MOV may cause loading and unbalance in the system.

C.1.1.2 Silicon semiconductor

These SPD components are formed from single or multiple PN junctions. Generally, these SPD components have a relatively low-energy handling capability and have temperature-sensitive characteristics. They are used where rapid voltage-limiting capability is required and can provide voltage protective levels of 1 V and greater. When used within their rated values, these components will have a high life expectancy. Exceeding device ratings usually results in catastrophic failure.

C.1.1.2.1 Forward-biased PN junction

A forward-biased PN junction diode (P-type silicon is positive in voltage with respect to the N-type silicon) has a threshold voltage (forward voltage, V_F) of about 0.5 V. Over most of the voltage-limiting range, the diode current increases rapidly with increasing applied voltage. Under high current conditions, the forward voltage may be over 10 V.

Under rapidly rising transient conditions, the diode may have some voltage overshoot. This overshoot (forward recovery voltage, V_{FRM}) may be comparable to or greater than the high current forward voltage. In the forward-biased polarity, the diode has a relatively high capacitance which is signal and dc level dependent. If the diode is normally reverse biased, then the working capacitance value is decreased, which may not cause a problem in high-frequency systems. Assemblies with series-connected diodes for higher operating voltages have a much reduced capacitance. The capacitance reduction is approximately in inverse proportion to the number of series connected diodes (e.g., five series connected diodes would have about one-fifth of the capacitance value of a single diode).

C.1.1.2.2 Avalanche breakdown device (ABD)

A reverse-biased PN junction diode (P-type silicon is negative in voltage with respect to the N-type silicon) in avalanche breakdown has a rated voltage [breakdown voltage, $V_{(BR)}$] of 7 V and greater. Over most of the voltage-limiting range, the ABD current increases rapidly with increasing applied voltage. Under high-current conditions, the limiting characteristic loops that result due to the resultant temperature increase, thus causing a corresponding increase in avalanche voltage.

The ABD has a fast response time, making it suitable to limit rapidly rising transient voltages. The capacitance of an ABD is dependent on the ac signal amplitude and dc bias. Also, the capacitance increases as the breakdown voltage decreases. To reduce the capacitance value for high-frequency systems, a forward biased diode can be connected in series with the ABD.

The single junction ABD is unidirectional. To make a bidirectional ABD, a second reverse-poled ABD can be connected in series. In each polarity, the functional elements are a series combination of an avalanching ABD and the second ABD operating as a forward-biased diode. As this is an NP to PN or PN to NP connection, it becomes possible to integrate the two ABDs into a single NPN or PNP structure.

C.1.1.2.3 Zener diode (regulator)

A reverse-biased PN junction diode (P-type silicon is negative in voltage with respect to the N-type silicon) in Zener breakdown has a rated voltage [breakdown voltage, $V_{(BR)}$] range of about 2.5 V to 5 V. Compared to the ABD, the zener has a voltage-limiting characteristic with a high slope resistance; a peak-limiting voltage of at least double the rated voltage may occur.

C.1.1.2.4 Punch-through diode

Punch-through diodes are NPN or PNP structures that use the widening center region depletion layer with increasing applied voltage to achieve conductivity between the space charge regions of the two PN junctions. Rated voltage levels of down to 1 V are possible. The punch-through diode was introduced as a replacement for zener diode regulators with lower limiting voltage and capacitance.

C.1.1.2.5 Foldback diode

Foldback diodes are NPN or PNP structures that use (NPN or PNP) transistor action to create a re-entrant voltage-limiting characteristic. Once the rated voltage is exceeded, the characteristic voltage decreases with increasing current to about 60% of the rated voltage. Higher levels of increasing current cause the characteristic voltage to increase. Compared to the equivalent ABD, the foldback diode has a lower limiting

voltage. The degree of foldback increases with rated voltage. For voltages in the 10-volt region, the degree of foldback is very small.

C.1.2 Voltage switching type

These SPD components have a discontinuous voltage-current characteristic. At a certain voltage-limiting level, these SPD components switch to a low-voltage state. In the low-voltage condition, the energy absorbed by a voltage-switching SPD will be less than a voltage-clamping type. In this low-voltage state, the power dissipated is low compared to that of other SPDs that "clamp" the voltage at a specific protection level. As a result of this switching action, protected equipment will be subjected to a voltage above the normal system voltage for only a very short time. Because of their switching action, these components may remain in a conducting state after the overvoltage has passed. Proper SPD selection and circuit design will allow SPD recovery to a high resistance state under normal system voltages and currents. (See Figure C.4 and Figure C.5.)

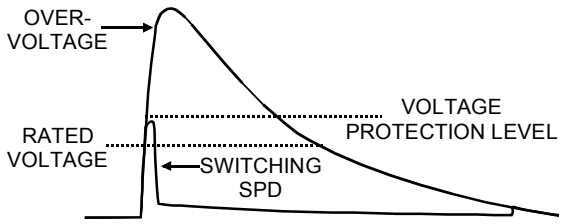

Figure C.4—Voltage-limiting of switching SPD

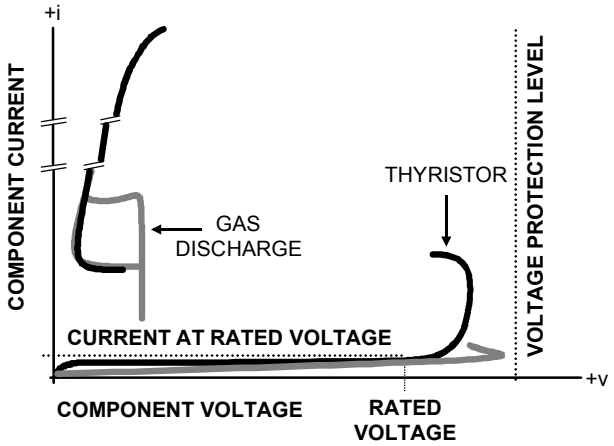

Figure C.5—Voltage-switching SPD characteristics for gas discharge and thyristor technologies

C.1.2.1 Gas discharge tubes

Gas discharge tubes consist of two or more metal electrodes, separated by a gap of less than 1 mm and held by a ceramic or glass cylinder. Noble gas or gas mixtures below and above atmospheric pressure fill the interior. When a slowly rising voltage across the gap reaches a value determined primarily by the gap size, gas pressure, and gas mixture, an ionization process begins. This process rapidly forms an arc between the two electrodes, with the residual voltage across the tube dropping to a value typically less than 30 V. The voltage at which this occurs is defined as the breakdown voltage of the gas tube.

If the applied voltage (transient) is rising rapidly, the time taken for the ionization/arc formation process may allow the transient voltage to exceed the value required for breakdown voltage in the previous paragraph. This voltage is defined as the impulse breakdown voltage and it generally is a positive function of the rate-of-rise of applied voltage.

Because of their switching action and rugged construction, gas tubes exceed other SPD components in current carrying capability. A 10-kiloamp peak with a waveform of 8/20 μ/sec can easily be carried by many types of gas tubes used in low-voltage systems applications.

The construction of gas tubes causes them to have very low capacitance, generally in the 2 to 3 pF range, a fact that allows their use in many high-frequency applications.

C.1.2.2 Thyristor surge protective device

These SPD components are formed from NPNP silicon structures. Inherently, these structures are unidirectional. To make a bidirectional device, a second PNPN structure is integrated in parallel. These SPD components have a relatively low-energy handling capability and temperature sensitive characteristics. As the majority of the diverted current is conducted in a low-voltage condition, a high-current capability results. When used within their rated values, these components will have a high life expectancy. Exceeding device ratings usually results in catastrophic failure.

C.1.2.2.1 Fixed-voltage thyristor SPD

A fixed-voltage thyristor SPD uses the breakdown voltage of the inner NP junction to set the rated voltage (see avalanche, zener, and foldback diode sections). This voltage is set in thyristor SPD manufacture and is typically 7 V and upward. Above a certain breakdown current, the NPNP structure regenerates and switches to a low-voltage condition. The peak value of breakdown voltage is called the breakover voltage [$V_{(BO)}$]. For the thyristor SPD to switch off, the current provided by the protected system must be below the thyristor SPD holding current, usually several hundred milliamperes. All thyristor SPD parameters are temperature sensitive, and this needs to be comprehended in the design.

Bidirectional thyristor SPD components can be symmetrical or asymmetrical. Unidirectional thyristor SPD components will only switch in one polarity. In the other polarity, the thyristor SPD may block current flow or conduct large current if a diode (PN junction) has been integrated in parallel. These unidirectional types provide benefits for certain applications.

The multiple PN junctions of the thyristor SPD reduce the overall capacitance. Values in the tens to hundreds of picoFarads are common. As with all PN junction devices, the capacitance is dependent on dc bias and signal amplitude. The breakdown voltage is dependent on the rate of rise of current. A power frequency ac rate of rise is used to determine the slow-rate breakover voltage. Under fast rates of rise, the impulse breakover voltage may be 10% to 20% higher.

C.1.2.2.2 Gated thyristor SPD

A gated thyristor SPD provides a gate connection to the central P or N regions of the NPNP structure. Connecting the gate to an external reference voltage sets the thyristor SPD-rated voltage to a similar value. This form of thyristor SPD is used where it is desirable to limit the overvoltage close to the external reference value. The external reference may be the supply voltage of the equipment electronics. P-gate types provide negative voltage protection, and N-gate types provide positive voltage protection. Bidirectional and unidirectional devices are available.

Annex D

(informative)

Thyristor SPD symbols

D.1 Thyristor SPD component symbols

Clause 5, Table 1 lists the many different types of thyristor SPD. In Clause 4, each type is shown in terms of basic silicon chip structure and the corresponding equivalent electronic circuit. Standard thyristor symbols do not cover this wide range of thyristor variants, nor do they identify the specific functionally of the thyristor SPD component. As a result, many manufacturers use their symbols to identify thyristor SPDs. This guide has tended to use boxes in circuit diagrams to signify thyristor SPDs to avoid confusion with specific manufacturers symbols. This clause shows some of the many different manufacturers symbols for thyristor SPDs.

D.1.1 Fixed-voltage thyristor SPD symbols

For this type of device the options, are blocking-unidirectional, conducting-unidirectional, symmetrical-bidirectional, and asymmetrical-bidirectional. A manufacturer's symbol for indicating an asymmetrical-bidirectional device has not been found. Asymmetrical device product information showed the symbol used for the more common symmetrical-bidirectional device. Each symbol has noted the number of manufacturers found using it. Unidirectional symbols are oriented to give the switching action with a positive potential applied to the top connector of the symbol.

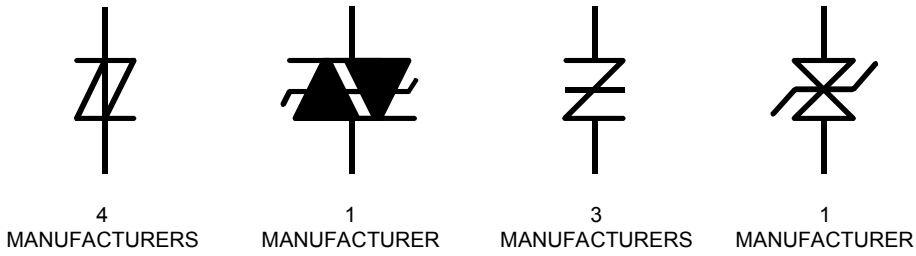

Figure D.1—Bidirectional symbols

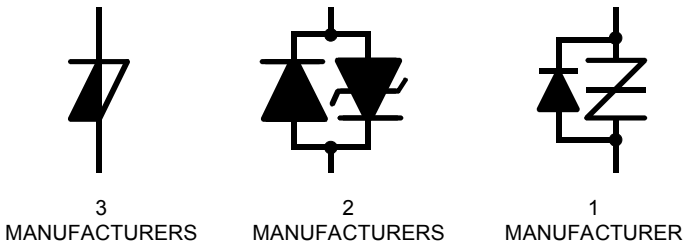

Figure D.2—Conducting-unidirectional symbols

3 MANUFACTURERS 1 MANUFACTURER

Figure D.3—Blocking-unidirectional symbols

D.1.2 Gated thyristor SPD symbols

For this type of device, the manufacturers tend to draw out the equivalent circuit of the device using standard symbols and not invent a unique symbol.